



Cantilever for Bio-Chemical Sensing Integrated in a Microliquid Handling System

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Cantilever for bio-chemical sensing integrated in a microliquid handling system

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Ph.D. Thesis
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30-06-2001

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Preface

This thesis has been written as a partial fulfillment of the requirements for obtaining the Ph.D.-degree at the Technical University of Denmark (DTU). The Ph.D.-project has been conducted at Mikroelektronik Centret (MIC) at DTU in the periode from January 1. 1999 to June 30. 2001.

The Ph.D.-project has been carried out at the Bioprobe project and has been supervised by the following people:

Project leader, Dr. Anja Boisen

Main supervisor for the project

Vicedirector of MIC, Dr. Francois Grey

Co-supervisor

The project has been financed by the FREJA programme within the electrical engineering programme at DTU.

The background for the project originated from the work presented by Anja Boisen in her Ph.D. thesis [1] from 1997. In this thesis the design and the fabrication of a piezoresistive AFM cantilever is presented. Based on this work I continued the work of the development of piezoresistive cantilevers for AFM in my Master's project. The thesis title is "Development of nano-probe with integrated readout and external probe scanner". After the end of my Master's project I joined the newly established Bioprobe project as a Ph.D student, with Anja Boisen as the project leader. The work performed in this project is described in this thesis.

Many people have contributed to and have been involved in the 2.5 years work of this project. My first first thank goes to my main supervisor and project leader Anja Boisen for a great collaboration during this project. Her enthusiasm and engagement in the work have been inspiring. I would also like to thank my supervisor and my former group leader, vice director Francois Grey for fruitful discussions.

A special thanks goes to Ole Hansen for countless creative ideas and suggestions especially within the development of the theory. It seems like he never runs out new ideas. I would also like to thank my former supervisor Siebe Bouwstra for introducing me to the exciting field of micro-technology. I am grateful for the the close collaboration I

have had with Peter Rasmussen who also work with the fabrication of cantilever-based sensors. My office mate during the last 2 years, Zachary Davis also deserves an acknowledgment for his friendship throughout. Eventhough he has not been working on the exact same subject, he has always been interested in my project. Rodolphe Marie has been an invaluable help during the DNA immobilization experiments. I would also like to thank the rest of the of the members of the Bioprobe project for very good fruitful discussions and pleasant company. I am grateful for the collaboration with Xiaomei Yu from University of Beijing during her stay at MIC. Her work on characterizing the $1/f$ noise and gauge factors of silicon has been very much appreciated. I would like to thank Erik Thomsen who has functioned as my supervisor in the final phase of this project. The lab technicians and process specialists at MIC have been a great support during my work in the clean room. I have received same high quality support from the administration group, and a special thanks goes to Lisbeth Thomsen and Anette Aakjær. During this project there have been both successes as well as disappointments, and I would like to thank Jamil El-Ali, Salim Bouaidat and Christian B. Nielsen for sharing them with me. A special thanks goes to the CS-team for sharing our common interests after working hours. I am also very grateful to the director of MIC, Jon Wulff Petersen for supporting this project. It has been a privilege to be able to work at MIC.

Last but certainly not least, I wish to express my deepest thanks to Fie and my family for their patience and support during this project.

Kgs. Lyngby, June 30. 2001

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Chapter 1

Introduction

The microfabrication technology is of increasing interest in modern science. Many opportunities in the technology are derived from down scaling of existing devices into the micrometer or even nanometer regime thereby obtaining better sensitivity or resolution. The technique also provides the opportunity to explore new basic scientific phenomena that occur at small dimensions. The most obvious example of the down scaling is found in microelectronics, while quantum confinement observed in nanostructures is a perfect example of a phenomena that cannot be observed in the macro-world.

The microfabrication technology has its basis in microelectronics, but during the eighties different groups began to fabricate micro electro-mechanical systems (MEMS) using the microfabrication technology [2]. Instead of making transistors and other electrical circuits, the microfabrication technology was used to build small 3-dimensional mechanical structures. An example of such a MEMS device is the accelerometer used in the airbag systems in cars [3]. The MEMS activity opened up for a whole new dimension of possibilities of using microfabrication, from simple down scaling of devices for performance optimization to exploring mechanical behaviors which are not observed in the macro-world. An example is the thermal actuation principle, which cannot be used in the macro-world due to its very large thermal time constant in bulky materials. But when the dimensions decreases to the micrometer regime, the thermal time constant decreases to microseconds or even smaller [4].

A very promising field of research within the microfabrication technology is devices for fluid handling. A. Manz *et al.* [5] was one of the first to work with this type of systems, and therefore his term "Micro Total Analysis Systems" (μ TAS) is being used to identify these structures. A μ TAS ideally is a system in which all steps from sample preparation to data representation are integrated in one instrument. The idea is actually to miniaturize a whole laboratory down on the chip, and the μ TAS concept is therefore also called "Lab on chip", see figure 1.1. The advantage of the μ TAS systems over conventional systems is found in small size, portability, low power consumption, low sample and reagent consumption and better performance in terms of sensitivity and measurement time.

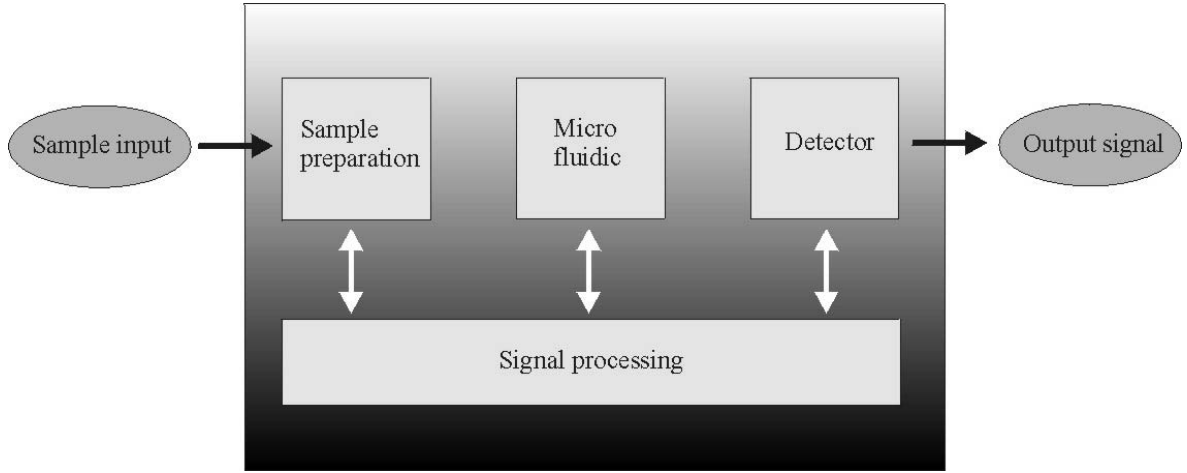


Figure 1.1: Elements in a micro total analysis system (μ TAS).

A lot of different detector mechanisms have been integrated into micro liquid handling systems. The detector principle is ranging from electrical sensing, as for example the ISFET [6] and the micro-electrodes for conductometric biosensing [7] over the electro-mechanical sensing, as for example the quartz balance [8] to the optical readout system by for example labeling of molecules with a fluorescent marker [9].

Labeling of molecules with fluorescent markers is a widely used technique within the field of biochemical sensing [10] and also the most commonly used technique within the μ TAS field [11]. The principle is based on attachment of a fluorescent group to the molecule of interest. As an example consider an antibody attached to a surface. A sample is brought in contact with the antibody coated surface and if the matching antigen is present in the sample it will bind to the antibody on the surface. After a washing step, fluorescent molecules, which only binds to the antigen, are brought in contact with the substrate, and they thereby bind to the antigen. The molecules on the substrate are now detected by shining a laser on the surface, and a fluorescent signal is picked up in a laser diode. The fluorescent signal intensity is concentration dependent, see figure 1.2. This detection method method is very sensitive and can

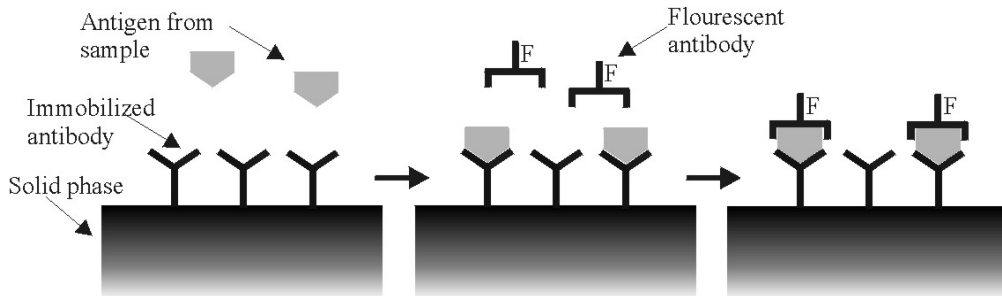


Figure 1.2: Schematic of molecules detection by fluorescent labeling

ultimately measure down to one single fluorescent group [12].

1.1 Cantilever-based sensor

In this thesis a cantilever-based biochemical sensor is described. The sensor mechanism is purely mechanical. The mechanical signal obtained from the cantilever can be translated into an electrical signal by use of a piezoresistive element. As will be described later, the detection method is very sensitive and fulfills the μ TAS requirement of integrated readout which many optical readout systems lack.

The background for using cantilever-based sensors is found in the atomic force microscope (AFM) invented by Binnig *et al.* in 1986 [13]. In AFM the force between a sample and a very sharp tip can be measured by detecting the bending of a cantilever with the tip attached to the end. In principle the method is the same as a miniaturized phonograph, see figure 1.3. A cantilever with a sharp tip at the end is moved across a sample surface and interatomic forces between tip and surface causes the cantilever to deflect. Usually, the cantilever deflection is used as a measure of surface topography and by scanning the tip relative to the surface, high resolution 3-dimensional topography image can be obtained.

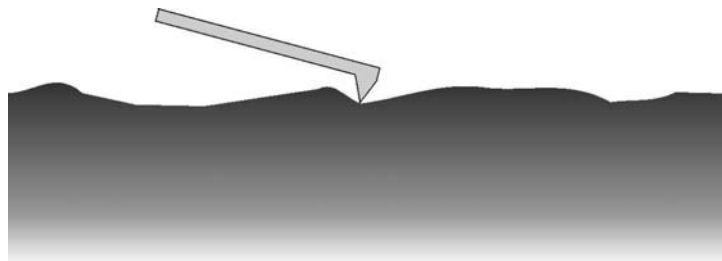


Figure 1.3: *Schematic of the AFM principle. The sharp tip attached to the cantilever follows the surface of the sample, and the cantilever bending is a measure of the surface topography.*

The bending of the cantilever can be detected by various kinds of readout systems. The most commonly used readout system is the optical leverage principle. The optical readout system consists of a laser and a deflection sensor, see figure 1.4. The laser beam is focused on the backside of the cantilever, and reflected onto a position sensitive laser diode. When the cantilever changes its deflection, the laser beam is reflected onto a different spot on the deflection sensor. A minimum detectable cantilever deflection of approximately 0.1 nm is normally obtained [14, 15].

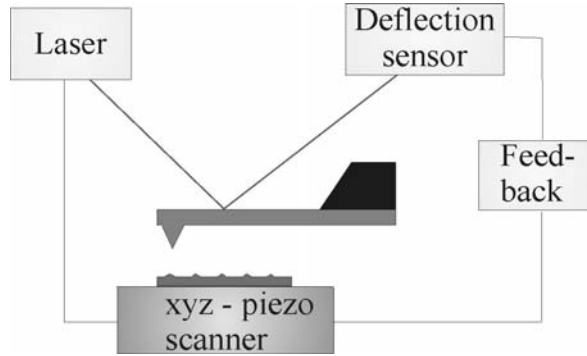


Figure 1.4: The AFM setup with optical readout and feedback loop. The tip-sample separation can be kept constant by means of the feedback system.

1.1.1 Piezoresistive AFM cantilevers

The optical readout system for detection of the cantilever deflection has certain disadvantages. A very accurate adjustment and alignment of the external laser and sensor with respect to the cantilever is necessary. Because of the difficulties in the cantilever alignment and the large mass of the laser system, it is often more convenient to scan the sample instead of the cantilever when doing AFM imaging. The sample is then placed on a piezotube, which limits the scanning range significantly. Furthermore, the use of optical readout under specific environmental conditions, e.g. ultra high vacuum (UHV) and low temperatures, is connected with an extensive and complicated experimental setup.

The disadvantages of an external sensor system may be avoided by integrating a deflection sensor onto the cantilever chip. Different detection schemes have been reported in the literature. These are *piezoelectric* [16, 17], *capacitive* [18] and *piezoresistive*.

We have chosen piezoresistive readout mechanism to be the best candidate as an integrated deflection sensor [1, 19]. This is mainly due to high flexibility of readout method with respect to scan environments and scanning modes. The piezoresistive readout can for example be applied in liquids, at low temperatures and in dusty environments.

Different groups have reported on the fabrication and applications of AFM cantilevers with piezoresistive readout. The first cantilever with piezoresistive readout was reported by Tortonese *et al.* [20] in 1991. They reported on a very simple cantilever design without tip. Since then, different approaches have been used to fabricate cantilevers with improved performance. There has been efforts in increasing the scanning speed by optimizing the dimensions [21, 22, 23], or optimizing the cantilever dimension in order to perform AFM scanning with atomic resolution [24]. Other groups have tried to optimize the performance of the cantilevers by changing the number of piezoresistors on the cantilever [25, 26]. Cantilevers with piezoresistive readout applied in UHV have been described in [27] and at low temperatures in [28]. Akiyama *et al.* [29] described

a piezoresistive cantilever for the use in outer space whereas Thaysen *et al.* [30] describes fully encapsulated piezoresistors for use in liquids. Finally, there have been a large amount of papers describing piezoresistive cantilevers with new *on chip* features. For example, Lange *et al.* describes a cantilever with integrated pre-amplifier [31] and Despont *et al.* [32] describes a dual-cantilever system for coarse and fine imaging.

The work presented in the literature regarding cantilevers with piezoresistive readout indicates that the obtainable resolution by using piezoresistive cantilevers in AFM is nearly as good as the resolution obtainable with optical readout [24, 33]. As will be described later, piezoresistive readout for cantilever-based biochemical sensing has not been described in details in the literature but is still believed to be a very strong candidate as the best readout technique.

1.2 Cantilever-based biochemical sensor

A new field of interest is to use AFM type cantilevers as very sensitive biochemical sensors. The cantilever surface is used as the "sensor" area in contrast to the AFM cantilever where the tip is used as the sensor part. Three principles have been used as detection schemes, see figure 1.5. A biochemical reaction on the cantilever surface

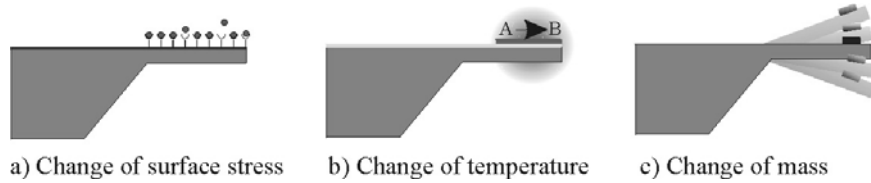


Figure 1.5: The three detection principles for biochemical sensing. a) illustrates changes in surface stress due to a chemical reaction. b) is illustrating the bending of a bimorph cantilever as a function of heating and c) shows the change in resonance frequency due to a mass change.

can be monitored as a bending of the cantilever due to a change in surface stress (a) or due to a temperature change (b). A temperature change can be detected by using a sandwich layered cantilever and thereby take advantage of the bimorph effect. Finally, it is possible to investigate mass changes on the cantilever by measuring the change in resonant frequency (c).

Although the generation of a surface stress (figure 1.5a) has been observed from biomolecular interactions, the origin of the surface stress change is still not understood and is probably very dependent on the specific molecular interaction.

1.2.1 Measurements performed with optical readout

Optical readout systems are the most commonly used detection principle since the cantilever-based biochemical sensing scheme originates from the AFM. It is relatively

easy to rebuild the AFM into a setup for biochemical sensing. Since no scanning is performed a scanner is not included in the experimental setup.

An example of measuring the change in temperature (1.5c) during a chemical reaction is reported by J. Gimzewski *et al.* [34]. Silicon cantilevers coated with a thick aluminum layer and a thin platinum layer have been used for measuring the heat formation during the catalytic conversion of $H_2 + O_2$ to form H_2O on the thin Pt layer.

In most of the published work concerning cantilever-based biochemical sensing the change in surface stress principle has been used, see figure 1.5a. For example, Thundat *et al.* [35] report on a cantilever coated with an ultra-violet cross-linking polymer used as a sensitive optical UV-radiation dosimeter. When exposed to radiation, the polymer coated cantilever bends due to stress obtained in the cross-linked polymer film. The cantilever bending is measured by optical detection technique.

The change in surface stress principle has also been used for characterization and identification of hydrogen chemisorption on a platinum surface [36, 37]. The chemisorption process is investigated at different temperatures and pressure conditions.

Detection of alcohols in gases has been performed by coating a cantilever with a polymer layer. An alcohol is introduced into a reaction chamber whereafter the evaporated alcohol is detected by a change in the polymer volume, which causes the cantilever to bend [38].

R. Berger *et al.* [39] have reported on change in surface stress during the formation of self-assembled alkanthiol layers in the gas phase on gold coated cantilevers. The self-assembled monolayer causes a compressive surface stress formation which closely follows a Langmuir-type adsorption model. The surface stress at monolayer coverage was found to increase linearly as a function of the length of the molecule.

O'Shea *et al.* [40] and Brunt *et al.* [41] report on a cantilever type sensor for electrochemical studies. The metal-coated cantilever is placed in a liquid cell. When applying a potential between a reference electrode and the cantilever metal a large change in surface stress is produced causing a bending of the cantilever due to changes in the electrolyte environment.

Fritz *et al.* [42] and Wu *et al.* [43] report on detection of hybridization of DNA complementary target oligonucleotides onto single stranded DNA oligonucleotides by optical detection. Gold coated cantilevers are first functionalized with thiolated probe DNAs and by later exposing the cantilever to the complementary DNA a surface stress change is observed. The articles also report on discrimination of single-nucleotide mismatches. The change in surface stress is found to be dependent on both the used buffer and the length of the target DNA oligonucleotide [42].

For DNA hybridization on the cantilever surface, it has been suggested that the surface

stress is obtained by electrostatic interactions between the molecules [39]. Another, more convincing explanation is given by Wu *et al.* [43]. They claim that both electrostatic interactions and changes in the entropy influences the change in surface stress. The single-stranded DNA molecule immobilized to the surface is very flexible but when the complementary part of the DNA molecule is hybridized, the new double-stranded DNA molecule becomes more stiff and ordered, which reduces the entropy. In [43] Wu *et al.* perform some experiments that indicates this theory, but more experiments have to be performed in order to develop a good theory.

The mass change sensing principle (see figure 1.5c) has been used for a sensitive alcohol detection [44, 45, 46]. The resonating cantilever is coated with a thin polymer layer. When exposed to an alcohol gas, the polymer layer absorbs the alcohol molecules and the polymer changes its mass. This mass change is observed as a change in the resonance frequency of the cantilever.

Other work performed using cantilever based biochemical sensors includes measurements on living cells [47] and specific antibody/antigen detection [48, 49]. Finally, interesting work has been done on investigating a protein's conformational changes [50] and pH stress change dependency of protein bovine albumin binded to the cantilever surface [51].

1.2.2 Measurements performed with piezoresistive readout

Cantilever-based biochemical sensing has also been performed by using cantilevers with piezoresistive readout. Berger *et al.* [52] report on the detection of mass changes during thermally induced dehydration of copper-sulfate-pentahydrate. The change in resonant frequency of the cantilever is measured by the integrated piezoresistor.

Alcohol detection in gases has been performed on a polymer coated cantilever by H. Jensenius *et al.* [53]. An alcohol is introduced into a reaction chamber whereafter the evaporated alcohol is detected by a change in the polymer volume, which causes the cantilever to bend.

Piezoresistive cantilevers have also been used for the detection of alkanethiol monolayer formation on gold coated cantilevers in gases by A. Hansen *et al.* [54]. The observed amplitude of the signal is very dependent on the surface roughness of the gold.

A. Boisen *et al.* [55] have reported on the change in surface stress as a function of ethanol concentration in water by use of piezoresistive readout. Finally, R. Marie [56] and Thaysen *et al.* [57] reports on the detection of the immobilization of the thiolated DNA oligonucleotides onto a gold surface and has shown a strong layer formation dependency on the used DNA concentration.

The results presented above indicates the variety of systems the cantilever based biochemical sensor has been tested on with both optical readout and piezoresistive read-

out. The sensitivity of the sensor has shown to be very high. Temperature changes down to 10^{-5}°C [34] have been resolved, and changes in the surface stress on the order of 10^{-5} N/m are measurable [58]. Finally, mass changes in the sub-nanogram regime have been resolved under ambient conditions [59].

The high sensitivity and the promising published results on cantilever-based sensor applications indicate that the cantilever based biochemical sensor is a strong candidate for a very simple and easy to use molecular detection scheme.

1.2.3 Piezoresistive readout vs. optical readout

Optical readout for a cantilever based biochemical sensor has some disadvantages, especially when applied in liquid. New alignment of the laser system with respect to the cantilever has to be performed every time the refractive index of the liquid changes. This might happen every time a different sample is introduced into the reaction chamber, see figure 1.6. Measurements with optical readout in non-transparent liquids, such

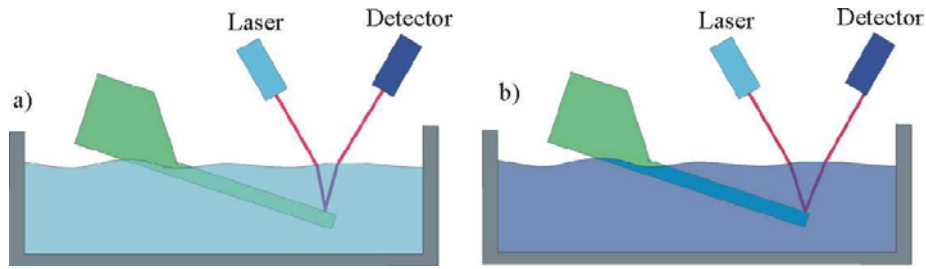


Figure 1.6: When the refractive index of the liquid in the reaction chamber is changed, a new laser alignment with respect to the cantilever has to be performed. The schematics show the influence of the refractive index on the lasers focus point on the cantilever. a) Focus point of the laser in a liquid, b) focus point of the laser when the refractive index of the liquid is changed

as for example blood, is not possible when using the optical readout technique, since all the laser light is absorbed in the liquid, see figure 1.7.

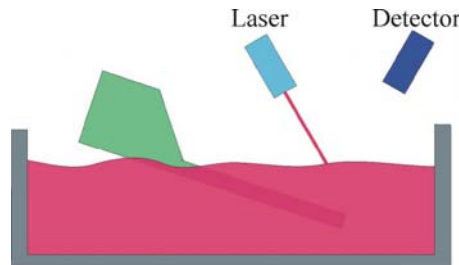


Figure 1.7: The schematic shows that it is impossible to obtain a signal from an external optical readout system when measuring in a non-transparent liquid.

It is often desirable to be able to read out from multiple cantilevers functionalized with different detector layers simultaneously. This is for example an advantage when using non-specific polymer coated cantilevers as an alcohol sensor [38]. The signal from one polymer-coated cantilever is here not enough to identify the actual alcohol and the concentration and thus more cantilevers coated with different polymers are required. Also, in the specific detection of biomolecules such as DNA strands and antigens, it is very interesting to be able to monitor several molecules simultaneously. In diagnostics, for example, one often needs to be able to detect more than one type of molecules. Using an optical readout system it becomes complicated with more than a couple of cantilevers. A multiplexing scheme has been used for solving this problem [38], however the alignment of the system becomes more and more difficult as the in number of cantilevers increases.

These problems are solved when using piezoresistive readout. No alignment of the is needed since the readout mechanism is *on chip*. The change in liquid and thereby the refractive index in the interaction chamber has no influence on the readout mechanism, and also measurements in non-transparent liquids can be performed, see figure 1.8. Since the signal from the piezoresistive readout system is a simple electrical signal, it is easy to expand one cantilever into an array of several cantilevers without any significant change in the setup. Finally, it is possible to design a very compact detector system by using piezoresistive readout and thereby obtaining a serious candidate as a *point of care* instrument.

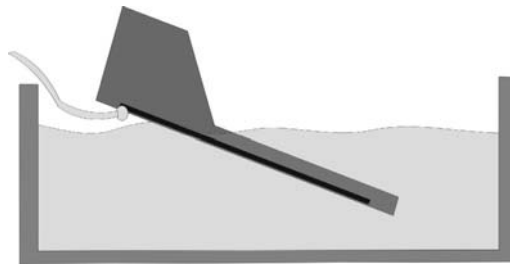


Figure 1.8: The schematic shows a piezoresistive cantilever in a liquid. The readout is no different from the readout in air except for the protection of the electrical connections

Due to the reasons mentioned above, the readout mechanism used in this thesis is chosen to be piezoresistive. To the author's knowledge, only the piezoresistive cantilevers fabricated and used at MIC during this thesis period have been operated on liquid [55, 56, 57]. The reason why this area is still uncovered is probably due to leak-current problems, and encapsulation of the electrical connections when using the cantilevers in liquids. Most of the cantilevers reported on in the literature are silicon cantilevers with diffused piezoresistor. When measuring in an electrolyte and no insulating and diffusion barrier layer is used for coating the piezoresistor, a severe leak current will run

into the electrolyte and thereby destroy the measurements. It is therefore necessary to carefully design cantilevers with completely encapsulated resistors when applying these into liquids. As will be described later, one of the goals of this thesis is to design and fabricate cantilevers that can be operated in liquid.

1.3 Other applications for cantilever based sensors

In this section a short overview of some other exciting areas where cantilever based sensors have been used is presented. The discussion will concentrate on cantilevers with piezoresistive readout.

1.3.1 Cantilever based data storage

Cantilever-based data storage is an interesting alternative to conventional magnetic data storage due to its potential high density improvement. The concept was first tested and published by Mamin *et al.* [60], where a conventional AFM tip with optical readout was heated in order to form a hole in a polymer film. The technique was transferred into cantilevers with integrated piezoresistive readout and the writing was performed by a integrating a heater on the tip heater [61]. Recently, Binnig *et al.* have demonstrated storage densities of up to 500 Gbit/in² by thermalmechanical writing in a thin polymer film with bit sizes and pitches of 20-30 nm each [62]. This is about 40-50 times more than today's best research demonstration with magnetic recording [63].

However, the reading and writing speed from a single cantilever is not competitive for data storage. For example, the highest data rate achieved with a single cantilever is 6 Mbit/s [22]. Using arrays of several hundreds or thousands of cantilevers operated in parallel, the cantilever based data storage can be improved significantly. IBM Research Laboratory in Zurich have reported on first a 5x5 cantilever array with read/write functions [64] and then a very high density array consisting of 32x32 cantilevers, called the Millipede [65, 66]. Instead of using piezoresistive readout, the reading is performed by measuring the heat transport from the cantilever as a function of the cantilever position, see figure 1.9.

Another approach to the cantilever based data storage system is presented by Chui *et al.* [68, 69] where a lateral deflection sensor is integrated in the cantilever in a highly inventive fabrication step. The lateral deflection sensor can then be used for tracking of the bits for higher performance and easier alignment.

1.3.2 Cantilever based lithography

Scanning probe lithography is an emerging area of research in which the AFM is used to pattern nanometer-scale features. Since the microelectronic industry continuously

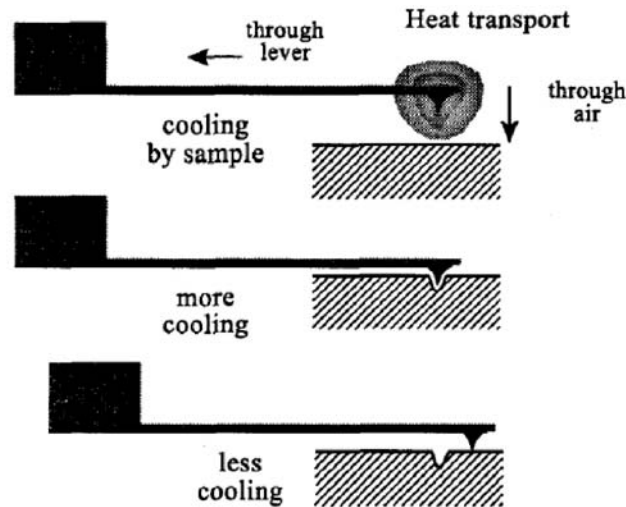


Figure 1.9: Reading mechanism of cantilevers in the Millipede concept [67].

pushes the limits for the line width, new methods for nanoscale lithography are explored. Mechanical patterning methods such as scratching or nanoindentation, and local heating with the sharp tip can be used as a lithography method. Another patterning principle is obtained when a voltage bias is applied between the sharp probe tip and the sample. An intense electrical field is generated in the vicinity of the tip, which can be used to locally oxidize for example a silicon surface or to expose an electron sensitive polymer. It is very important that the cantilever is able to scan over a very large area and with high speed in order to be a serious candidate for the next generation lithography technique. It is therefore again necessary to design arrays of cantilevers in order to obtain high writing speed.

Chow *et al.* report on a two dimensional piezoresistive cantilever array with integrated through-wafer interconnections for imaging or lithography [70]. Minne *et al.* reports on a cantilever array scanning an area of 100 mm² [71].

The technique is still far from being so mature that it can compete with the existing optical lithography. However, there might be applications where the technique can be used at this stage.

1.4 The Bioprobe project

The Bioprobe project at MIC deals with cantilever-based sensors with piezoresistive readout for biochemical detection. Cantilevers with piezoresistive readout and fully encapsulated resistors have already been fabricated and used for AFM at MIC [1, 19]. The Bioprobe project was initiated in January 1999 and the aim of the project is to use cantilevers in liquid surroundings for the investigation of specific biochemical reactions

on the cantilever surface.

One of the major challenges of the Bioprobe project is to realize cantilevers with piezoresistive readout which can be operated in liquid and which are sensitive enough for detection of the biochemical reactions.

As described previously, most groups working with cantilever based biochemical sensors use optical readout as detection principle. The cantilever is placed in a commercially available liquid cell with a volume on the order of hundreds of microliters. The large volume increases the reaction time significantly since the diffusion of the molecules from the liquid onto the cantilever surface determines the reaction rate. The liquid cell volume is furthermore so large that thermal gradients can be obtained in the cell which increases the drift of the system. The volume size also allows turbulence to exist, which might cause the cantilever to vibrate, and thereby increase the noise level.

These negative effects of using a liquid cell, can be avoided by integrating the cantilever into a micro liquid handling system. The interaction chamber in such a device is typically on the order of $0.1\ \mu\text{L}$, and the diffusion time of the molecules to the cantilever is reduced. Due to the small volume, temperature gradients are also minimized and finally strictly laminar flows are obtained in micro liquid handling systems. Since it is normally an advantage to measure several biochemical entities simultaneously, it has been decided to build an array of 10 cantilevers into the micro liquid handling system.

1.5 Overview of this thesis

The aim of this project is to design, fabricate, characterize and use an array of cantilever based biochemical sensors integrated in a micro liquid handling system. The detection principle is chosen to be piezoresistive readout. The thesis will focus mostly on the design and fabrication of such a chip, and it will only be used in simple applications. The reason for this is that more difficult applications is out of the scope of this thesis, but will be described in other works from the Bioprobe project.

In this thesis three topics are completely new with respect to previously published work in the field of cantilever-based biochemical sensor:

- A new theory has been developed which explains the behavior of a piezoresistive cantilever exposed to a surface stress
- Optimization of the piezoresistor material parameters in order to design very sensitive cantilever based biochemical sensors.
- Designing and fabrication of a cantilever based biochemical sensor integrated into a micro liquid handling system

1.5.1 Outline of chapters

- In Chapter two a general theory for the behavior of a cantilever subjected to a stress is presented. The theory also describes the noise sources.
- Chapter three deals with the optimization of the resistor material with respect to high sensitivity. This is done, first by presenting the characterization of the materials and then the signal to noise ratio is calculated.
- The design of the chips is described in Chapter four, which takes the theory, parameter optimization and the fabrication considerations into consideration.
- Chapter five discusses some of the fabrication considerations in order to obtain a simple fabrication sequence for the chip.
- Chapter six describes the processing of the chip. Two versions of the fabrication process are described. The second version takes some of the mistakes found in version one into considerations.
- The chip is characterized in Chapter seven with respect to sensitivity and noise.
- In Chapter eight the experimental setup for the use of the chip is discussed. Several applications of the chip are discussed.
- Finally, Chapter nine concludes this thesis with the most important achievements and results.
- Appendix A includes the list of published articles during this project.
- In Appendix B a short version of the fabrication process of the chip is presented
- The English summary of the thesis is given in Appendix C and the Danish summary in Appendix D.

Chapter 2

Theory

In this chapter the theoretical considerations, which are used for understanding the mechanics of a piezoresistive cantilever are presented. The conclusions drawn from this chapter will make it possible to design cantilevers optimized for specific applications. First, the basic mechanics, such as resonant frequency and spring constant for a cantilever is presented. Then the principles of end-point deflection sensitive cantilevers with piezoresistive readout are described. This type of cantilevers are for example used in AFM. The results from this part are used to determine the gauge factor from end-point measurements. Hereafter a theory for a surface stress sensitive cantilever with piezoresistive readout is presented. This part does also describe the bending of a composite cantilever with build-in stress. Finally, the most important noise contributions, originating from Johnson noise, Hooge noise and thermal vibrational noise are calculated. These noise contributions determine the obtainable resolution with the cantilever.

2.1 Basic mechanics

The most basic mechanic parameters of a cantilever is the spring constant and the resonant frequency. These parameters are very important for the use in AFM [72] but not so important for surface stress sensing with piezoresistive readout. Still, it is important to have these parameters in mind when designing the sensor, since a too soft cantilever will simply bend due to its own weight and mechanical noise from the surroundings will excite the cantilever if the resonant frequency is too low.

The spring constant k is defined as the constant of proportionality between the bending of a cantilever z due to a applied force F . The relation is called Hook's law:

$$F = -kz \tag{2.1-1}$$

For a rectangular cantilever of length l the spring constant is

$$k = \frac{3EI}{l^3} \tag{2.1-2}$$

where E is Young's modulus and I is the moment of inertia. A typical spring constant for a stress sensitive cantilever is normally in the range between 1 mN/m and 1 N/m.

The resonant frequency, f_{res} , for a simple rectangular cantilever can be expressed as [72]

$$f_{res} = 0.162 \frac{\sqrt{E} h^3 w}{\sqrt{\rho} l^2} \quad (2.1-3)$$

where ρ denotes the mass density, h the cantilever thickness and w denotes the width of the cantilever. For stress sensitive cantilevers the resonant frequency should normally be higher than 5 kHz, in order to reduce the influence of the noise from the surroundings. Using the moment of inertia for rectangular cantilever [72]

$$I = \frac{wh^3}{12} \quad (2.1-4)$$

and the mass which can be expressed as $m = lwh\rho$, a relation between the resonant frequency and the spring constant can be obtained as

$$f_{res} = 0.32 \sqrt{\frac{k}{m}} \quad (2.1-5)$$

This relation shows that the resonant frequency increases as a function of increasing spring constant. For AFM type cantilevers it is normally desirable to obtain a high resonance frequency ($f_{res} > 100$ kHz) and a low spring constant ($k < 1$ N/m). It is seen from the relation 2.1-5 that this can be obtained by using a low mass m of the cantilever, thus small dimensions.

The cantilever described in this thesis consists of a composite structure. It is not possible just to add the moment of inertia described in equation 2.1-4 for the different cantilever layers in order to find the resulting moment of inertia for the composite cantilever. It is necessary to introduce a parameter called the neutral axis, denoted z_N . The neutral axis defines a position in the cantilever where there is no stress in the cantilever when bent. For example, figure 2.1 shows the neutral axis in a cross-sectional view of a cantilever, when it experiences a point-force F at the apex of the cantilever. A tensile stress is obtained at the top of the cantilever, while the backside experience a compressive stress. The neutral axis z_N is defined as

$$z_N = \frac{\sum_i E_i z_i h_i}{\sum_i E_i h_i} \quad (2.1-6)$$

where z_i is the position of the i 'th-layer and h_i the thickness of the i 'th layer. The moment of inertia I_i of the i 'th layer is defined as

$$\begin{aligned} I_i &= \int_A y^2 dA \\ &= \int_{z_i - z_N - h_i/2}^{z_i - z_N + h_i/2} y^2 w dy \\ &= \frac{wh_i^3}{12} + wh_i(z_i - z_N)^2 \end{aligned} \quad (2.1-7)$$

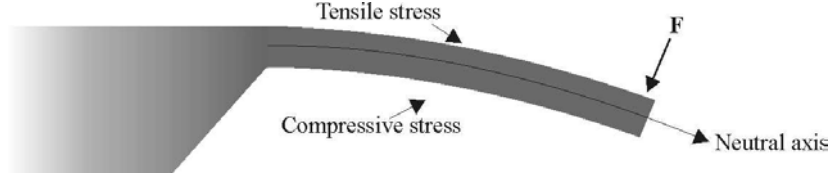


Figure 2.1: Cross-sectional schematic of a cantilever experiencing a point-force at the apex of the cantilever. A tensile stress is obtained at the top of the cantilever and a compressive stress is obtained at the backside of the cantilever. The neutral axis is defined as the position, where no stress is observed.

where A is the cross sectional area, y is the distance to the neutral axis and $z_i - z_N$ is the distance between the center of the i th layer and the neutral axis. The effective stiffness EI for the composite cantilever can now be expressed in the following way by summing over all the products of Young's modulus and moment of inertia of each layer

$$EI = w \sum_i (E_i (\frac{h_i^3}{12} + h_i (z_i - z_N)^2)) \quad (2.1-8)$$

This expression can then be used in 2.1-2 to find the spring constant for a composite cantilever and in 2.1-5 to find the resonant frequency for the cantilever.

2.2 End-point deflection sensitive piezoresistive cantilever

As described in the introduction, the cantilevers with piezoresistive readout developed previously at MIC [1, 19, 73] were designed to be used in AFM and were therefore optimized to be sensitive to a deflection of the apex of the cantilever. This section deals with the theory concerning the sensitivity of such cantilevers. The main reason for describing this theory is that it is used during the characterization of the gauge factor of the piezoresistor. By comparison of the theory for end-point deflection sensitive cantilevers and surface stress sensitive cantilevers, it will be obvious that cantilevers optimized for end-point deflection sensitivity are not optimized for surface stress sensitivity and vice-versa.

A piezoresistor changes its resistance when strained. In this thesis only silicon piezoresistors are considered since they exhibit a very large piezoresistive effect, for example compared to metal [74]. The relative change in resistance as a function of strain ϵ can be written as

$$\frac{\Delta R}{R} = K_l \epsilon_l + K_t \epsilon_t \quad (2.2-1)$$

where K denotes the gauge factor, which is a material parameter and the subscripts l and t stand for longitudinal and transversal, respectively.

It is usually an advantage to minimize either the longitudinal or the transversal contribution to the strain since the gauge factors in the two directions have opposite signs in the case of silicon. In this thesis this is done by placing the resistor in a configuration where the resistance in the longitudinal direction is much larger than the resistance in the transversal direction, see figure 2.2. The sensitivity can be found by considering a

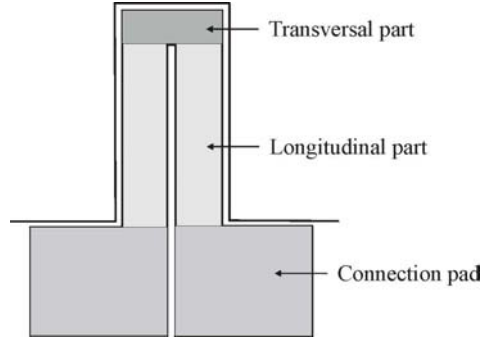


Figure 2.2: Schematic of a cantilever with integrated piezoresistor. The resistor is placed such that the transversal contribution can be minimized compared to the longitudinal contribution

piezoresistor with length λ , placed in a thin cantilever, see figure 2.3. The stress $\sigma(x)$

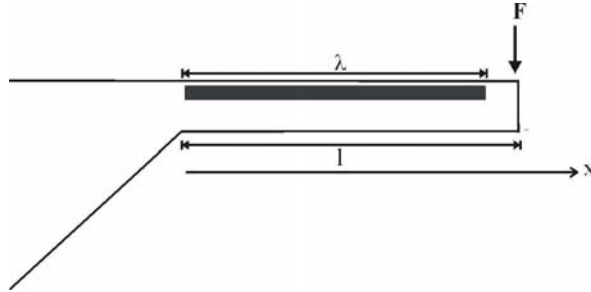


Figure 2.3: A cantilever with integrated piezoresistor with a length λ . The cantilever length is l and it is clamped at $x = 0$. The cantilever experiences a force F at the end of the cantilever

at a distance x from the clamped end of the cantilever is given by [75]

$$\sigma(x) = \frac{M(x)z_{NR}}{I} \quad (2.2-2)$$

where $M(x) = F \cdot (l - x)$ is the bending moment. F is the force acting on the apex of the cantilever, l denotes the cantilever length and z_{NR} is the distance between the resistor and the neutral axis. The average stress in the resistor is found by integrating over the length of the resistor

$$\langle \sigma \rangle = \frac{1}{\lambda} \int_0^\lambda \sigma(x) dx = \frac{F(1 - \frac{1}{2} \frac{\lambda}{l})l \cdot z_{NR}}{I} \quad (2.2-3)$$

Using that $\sigma = E\epsilon$ in equation 2.2-3 and inserting into the longitudinal part of equation 2.2-1, the sensitivity can be expressed as a function of the force F .

$$\frac{\Delta R}{R} = K \frac{(1 - \frac{1}{2} \frac{\lambda}{l}) l \cdot z_{NR}}{EI} F \quad (2.2-4)$$

This equation can also be written as a deflection sensitivity, using Hooke's law (equation 2.1-1)

$$\frac{\Delta R}{R} = -K \frac{(1 - \frac{1}{2} \frac{\lambda}{l}) l \cdot z_{NR} \cdot k}{EI} z \quad (2.2-5)$$

In order to measure an electrical signal instead of a change in resistance, the piezoresistor on the cantilever is placed in a Wheatstone bridge. This bridge converts the change in resistance into a voltage change, see figure 2.4. Assuming that $\Delta R \ll R$ the output signal V_{out} can be written as

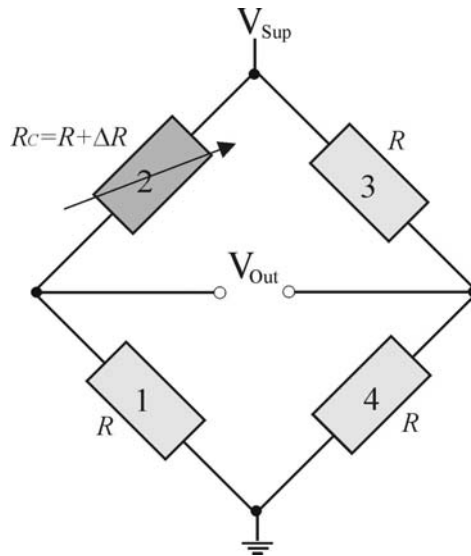


Figure 2.4: Schematic of a Wheatstone bridge. The cantilever resistor is denoted by R_C . The supply voltage is V_{sup} and the output voltage is V_{out} .

$$V_{out} = \frac{1}{4} \frac{\Delta R}{R} V_{sup} \quad (2.2-6)$$

where V_{sup} is the supply voltage. It is now possible to set up an equation for the deflection sensitivity for a cantilever where the piezoresistor is inserted in a Wheatstone bridge, by using equation 2.1-2, 2.2-5 and 2.2-6

$$\frac{V_{out}}{V_{sup}} = K \frac{3(1 - \frac{1}{2} \frac{\lambda}{l}) z_{NR}}{4l^2} z \quad (2.2-7)$$

From this equation it is seen that in order to make the cantilever as sensitive as possible, the resistor has to be short compared to the cantilever length. The resistor should be placed far away from the neutral axis and the cantilever should be designed as short as possible.

2.3 Stress in a cantilever

In this section the theory concerning the mechanics of a composite cantilever exposed to different kind of stresses is presented. The theory is developed in collaboration with O. Hansen [76]. First, a very general theory is presented, whereafter it is split up into sub-parts. The most relevant part is the derivation of the sensitivity to surface stress changes, since it is this phenomenon which is used in the biochemical sensing mechanism. The theory reveals some striking results which by the first impression seems counter-intuitive. Some simple examples are presented in order to give a better understanding of the surface stress sensing mechanism. The bending of the cantilever due to build-in stress in the cantilever layers can also be calculated from the theory and is also presented here.

2.3.1 General stress theory in a cantilever

The composite cantilever consists of i layers with thickness h_i , with built in stress σ_i and Young's modulus E_i . The built-in stress is partially relaxed leaving a strained bent cantilever. Since it is possible to superpose the deformations acting on a mechanical structure, the strain $\epsilon(z)$ in the cantilever can be expressed as a stretching/compression part ϵ_0 which is constant through the cantilever and a pure bending part, βz . β is a constant and z the distance to the neutral axis. Thus, the strain $\epsilon(z)$ can be expressed as

$$\epsilon(z) = \epsilon_0 + \beta z \quad (2.3-1)$$

The strain through the cantilever is visualized in figure 2.5. The uniaxial stress in the

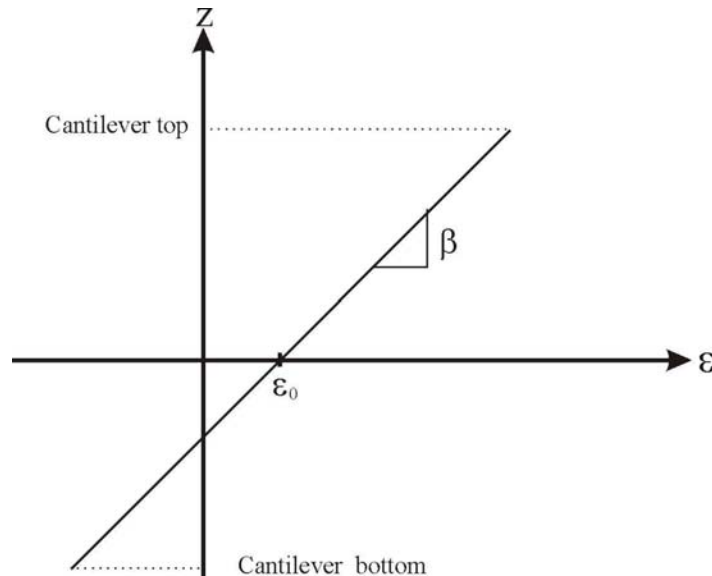


Figure 2.5: The strain ϵ as a function of position through the cantilever. The neutral axis z_N is positioned in $z = 0$. It can be seen that the stretching/compression strain off-sets the strain with respect to the neutral axis.

cantilever can be expressed as the build-in stress in the layers, σ_i , and the strain $\epsilon(z)$, (see expression 2.3-2)

$$\sigma(z) = \sigma_i + E_i \epsilon(z) \quad (2.3-2)$$

By inserting 2.3-1 in 2.3-2 the following expression for stress is obtained

$$\sigma(z) = \sigma_i + E_i \epsilon_0 + E_i \beta z \quad (2.3-3)$$

In order to obtain a cantilever in equilibrium the total force F acting on the cantilever has to equal zero. Since the width w of the different layers throughout the cantilever is kept constant, and since the stress can be expressed as $\sigma = F/A$ where A is the cross-sectional area, the force can be written as

$$\begin{aligned} F &= \int_{z_B}^{z_T} \sigma dz \\ &= \int_{z_B}^{z_T} \sigma_i dz + \int_{z_B}^{z_T} E_i \epsilon_0 dz + \int_{z_B}^{z_T} E_i \beta z dz \\ &= \sum_i \sigma_i h_i + \epsilon_0 \sum_i E_i h_i + \beta \sum_i E_i \frac{z_{iT}^2 - z_{iB}^2}{2} = 0 \end{aligned} \quad (2.3-4)$$

where z_T and z_B are the distances from the top and the bottom of the cantilever to the neutral axis, respectively, and $z_{iT} - z_{iB} = h_i$. The expression in 2.3-4 can be simplified since $z_{iT}^2 - z_{iB}^2 = (z_{iT} - z_{iB})(z_{iT} + z_{iB}) = 2h_i z_{iC}$, where z_{iC} defines the middle of the i th layer. The force balance 2.3-4 can now be expressed as

$$F = \sum_i \sigma_i h_i + \epsilon_0 \sum_i E_i h_i + \beta \sum_i E_i h_i z_{iC} = 0 \quad (2.3-5)$$

This expression can be simplified even more by taking the definition of the neutral axis into consideration, given in 2.1-6, where the distance z_i to the neutral axis from the layer, now is denoted by z_{iC} . From figure 2.5 it is seen that the neutral axis, is defined as $z_N = 0$. Inserting this, into the definition of the position of the neutral axis 2.1-6, the following requirement is obtained:

$$\sum_i E_i h_i z_{iC} \equiv 0 \quad (2.3-6)$$

Inserting 2.3-6 in expression 2.3-5, the uniform stretching/compression strain ϵ_0 can be expressed as

$$\epsilon_0 = -\frac{\sum_i \sigma_i h_i}{\sum_i E_i h_i} \quad (2.3-7)$$

The stretching/compression strain in the cantilever can now be determined if the build-in stress, thicknesses and Young's modulus of each layer are known.

Having defined the neutral axis to $z_N = 0$ the position of the top surface z_T with respect to the neutral axis can be found knowing the thickness of the individual layers.

The middle of the i th layer can be rewritten as a function of the position of the top surface and the individual layers as

$$z_{iC} = z_T - \sum_{j=0}^i h_j + \frac{h_i}{2} \quad (2.3-8)$$

This equation simply states that the middle of the i th layer, z_{iC} , can be expressed as the thickness of the layers between the i th layer and the top surface z_T subtracted from the position of the top layer.

By inserting 2.3-8 in equation 2.3-6 the following equation is obtained.

$$\sum_i E_i h_i (z_T - \sum_{j=0}^i h_j + \frac{h_i}{2}) \equiv 0 \quad (2.3-9)$$

Solving equation 2.3-9 with respect to z_T yields

$$z_T = \frac{\sum_i E_i h_i (\sum_{j=0}^i h_j - \frac{h_i}{2})}{\sum_i E_i h_i} \quad (2.3-10)$$

from which the position of the top surface layer with respect to the neutral axis can be calculated.

In order to find β from equation 2.3-1, the bending moment around the neutral axis has to be considered. Again, it is required that the total bending moment M has to equal zero. The bending moment is defined as

$$M = \int_{z_B}^{z_T} z \sigma dz \quad (2.3-11)$$

and inserting 2.3-3 in equation 2.3-11, the bending moment can be expressed as

$$\begin{aligned} M &= \int_{z_B}^{z_T} z \sigma dz + \int_{z_B}^{z_T} z \epsilon_0 E_i dz + \int_{z_B}^{z_T} E_i \beta z^2 dz \\ &= \sum_i \sigma_i h_i z_{iC} + \epsilon_0 \sum_i E_i h_i z_{iC} + \beta \sum_i E_i \frac{z_{iT}^3 - z_{iB}^3}{3} = 0 \end{aligned} \quad (2.3-12)$$

but since it is required that $\sum_i E_i h_i z_{iC} \equiv 0$ (see equation 2.3-6) the bending moment balance can be reduced to

$$M = \sum_i \sigma_i h_i z_{iC} + \beta \sum_i E_i \frac{z_{iT}^3 - z_{iB}^3}{3} = 0 \quad (2.3-13)$$

The $z_{iT}^3 - z_{iB}^3$ part can be written as

$$z_{iT}^3 - z_{iB}^3 = h_i (3z_{iC}^2 + (\frac{h_i}{2})^2) \quad (2.3-14)$$

and by inserting this in equation 2.3-13, β can be found to

$$\beta = -\frac{\sum_i \sigma_i h_i z_{iC}}{\sum_i E_i h_i (z_{iC}^2 + \frac{1}{3}(\frac{h_i}{2})^2)} \quad (2.3-15)$$

β can also be expressed as a function of the position of the top surface z_T , by inserting 2.3-10 into equation 2.3-15

$$\beta = -\frac{\sum_i \sigma_i h_i (z_T - \sum_{j=0}^i h_j + \frac{h_i}{2})}{\sum_i E_i h_i ((z_T - \sum_{j=0}^i h_j + \frac{h_i}{2})^2 + \frac{1}{3}(\frac{h_i}{2})^2)} \quad (2.3-16)$$

Inserting β from 2.3-16 and ϵ_0 from 2.3-7 in equation 2.3-1 gives an expression for the strain ϵ_z at any position in the cantilever as a function of the cantilever layers material parameters, dimensions and build-in stresses.

2.3.2 Pure surface-stress sensitivity

In this section the sensitivity to surface-stress change is derived from the theory given in section 2.3.1. In order to simplify the expression it is assumed that the build-in stress in all the cantilever layers equals zero. The assumption does not conflict with the real case where the build-in stress in the cantilever layers do not equal zero, since the forces acting on the cantilever can be superposed, and therefore build-in stresses in the layers will only act as an off-set.

Surface stress is defined by a stress in an infinitely thin layer. This requires that the height of the top layer $h_T = 0$ and $\sigma_T h_T = \sigma_s$ where σ_s is the surface stress, with dimensions $[N/m]$.

The strain ϵ_0 in equation 2.3-7 can now be written as

$$\epsilon_0 = -\frac{\sigma_s}{\sum_i E_i h_i} \quad (2.3-17)$$

and also the equation for β 2.3-16 can be simplified to

$$\beta = -\frac{\sigma_s z_T}{\sum_i E_i h_i \left((z_T - \sum_{j=0}^i h_j + \frac{h_i}{2})^2 + \frac{1}{3}(\frac{h_i}{2})^2 \right)} \quad (2.3-18)$$

In order to find the strain in the resistor layer, which is defined as layer R in the cantilever, the z in equation 2.3-1 has to correspond to the position of the resistor layer. This is defined as

$$z_R = z_T - \sum_{j=0}^R h_j + \frac{h_R}{2} \quad (2.3-19)$$

The full expression for the surface stress sensitivity ($\frac{\Delta R}{R}$) for a composite cantilever can now be expressed by inserting 2.3-19, 2.3-18 and 2.3-17 into equation 2.3-1. Then

this is inserted in the longitudinal part of equation 2.2-1, yielding

$$\frac{\Delta R}{R} = K \left(-\frac{1}{\sum_i E_i h_i} - \frac{z_T(z_T - \sum_{j=0}^R h_j + \frac{h_R}{2})}{\sum_i E_i h_i ((z_T - \sum_{j=0}^i h_j + \frac{h_i}{2})^2 + \frac{1}{3}(\frac{h_i}{2})^2)} \right) \sigma_s \quad (2.3-20)$$

This equation shows that the surface stress sensitivity is only dependent on the thickness of the layers, Young's modulus, and the distance between the neutral axis and the resistor layer. By comparison with the deflection sensitivity found in equation 2.2-5 it is seen that the surface stress sensitivity is not dependent on the length of the cantilever and the length of the resistor and its position. This means that stress will not be picked-up in the resistor in places where no surface-stress is detected. The surface stress sensitivity can therefore be considered local. This phenomenon is visualized in figure 2.6, where the cantilever exhibits constant curvature in places where a surface stress is induced, and the cantilever is straight where no surface stress is induced.

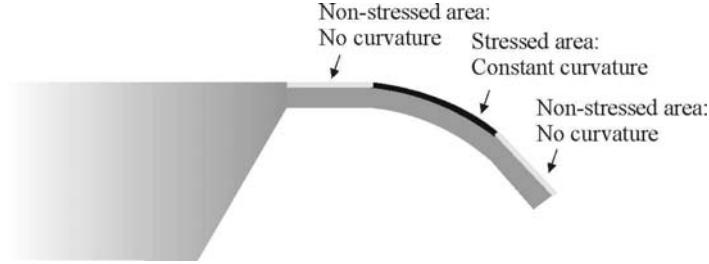


Figure 2.6: The cantilever exhibits a constant curvature in places where surface stress is applied and no curvature at places with no surface stress. Therefore the built-in piezoresistive sensor is only sensitive to local surface stress

2.3.3 Pure surface-stress in a simple cantilever

In this section an example of the surface stress sensitivity of a simple one layer cantilever is presented. This is done due to the rather complicated equation in 2.3-20 which does not give a full understanding of the surface stress sensitivity mechanics theory.

In this example a surface stress σ_s is induced in the top of the cantilever. The cantilever consists of one material with Young's modulus E and thickness h . The resistor is assumed to be infinitely thin placed at the top of the cantilever, see figure 2.7. Inserting this in equation 2.3-20, a very simple expression for the sensitivity is found

$$\left(\frac{\Delta R}{R} \right)_{RT} = -K \left(\frac{1}{Eh} + \frac{3}{Eh} \right) \sigma_s = -K \left(\frac{4}{Eh} \right) \sigma_s \quad (2.3-21)$$

since the neutral axis is placed at $\frac{h}{2}$. This expression is much simpler than the full expression. It is very clear from the expression that only the thickness and the

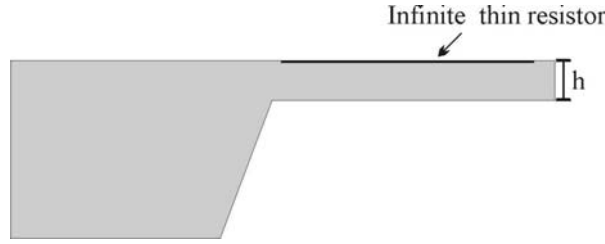


Figure 2.7: The cantilever consist of one material with Young's modulus E and thickness h . This resistor is assumed to be infinitely thin placed at the top of the cantilever

stiffness of the material influence the sensitivity. It can be seen from the expression that the stretching/compression strain ϵ_0 applies a relative strain in the resistor equal to 1 while the bending strain β applies a relative strain of 3. The effect of that is illustrated in figure 2.8, where the strain as a function of position in the cantilever is plotted. It is seen that due to the stretching/compression stress, the strain curve is off-set with respect to the neutral axis. The result of that can best be illustrated by

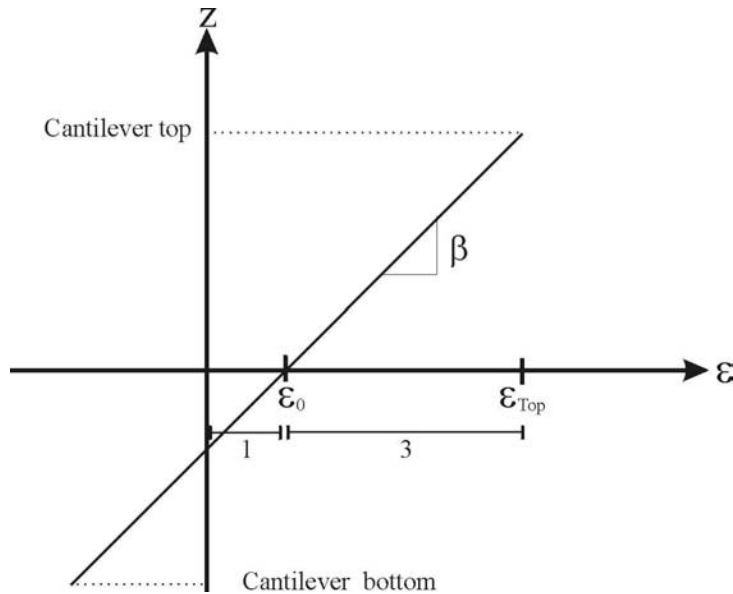


Figure 2.8: The graph shows a plot of the strain in the cantilever as a function of the position in the z -direction. It can be seen that the stretching/compression strain off-sets the strain with respect to the neutral axis

an example similar to the one above, where the resistor now is placed at the bottom of the cantilever. In terms of the top layer z_T the infinitely thin resistor is now placed at $z_T - h$. Inserting this in equation 2.3-20 the following expression for the sensitivity is obtained

$$\left(\frac{\Delta R}{R}\right)_{RB} = -K \left(\frac{1}{Eh} - \frac{3}{Eh}\right) \sigma_s = K \left(\frac{2}{Eh}\right) \sigma_s \quad (2.3-22)$$

It can be seen that the bending strain and the stretching/compression strain have opposite sign, and the resulting sensitivity is decreased by a factor of two. The reason for this behavior is illustrated in figure 2.9 where the behavior of a cantilever exposed to a compressive surface stress is split up into two phenomena; stretching and bending of the cantilever. The applied surface stress is denoted with the grey text while the resulting stress in the cantilever is denoted by the thick black text. Cantilever (a) in figure 2.9 is exposed to a compressive surface stress on both sides of the cantilever and therefore experiences a tensile stress in, or stretching of, the whole cantilever. Cantilever (b) is exposed to a compressive surface stress on the top side of the cantilever and a tensile surface stress on the backside of the cantilever. This results in a pure bending of the cantilever, with a tensile stress in the top of the cantilever and compressive stress in the bottom of the cantilever. The resulting behavior is obtained by "adding" the two phenomena, yielding a cantilever that only experiencing a compressive surface stress on the top side of the cantilever. The numerical value of the resulting tensile stress in top part of cantilever is larger ($a+b$) than the numerical value of the resulting compressive stress ($a-b$) in the bottom part of the cantilever. It is therefore very important to place

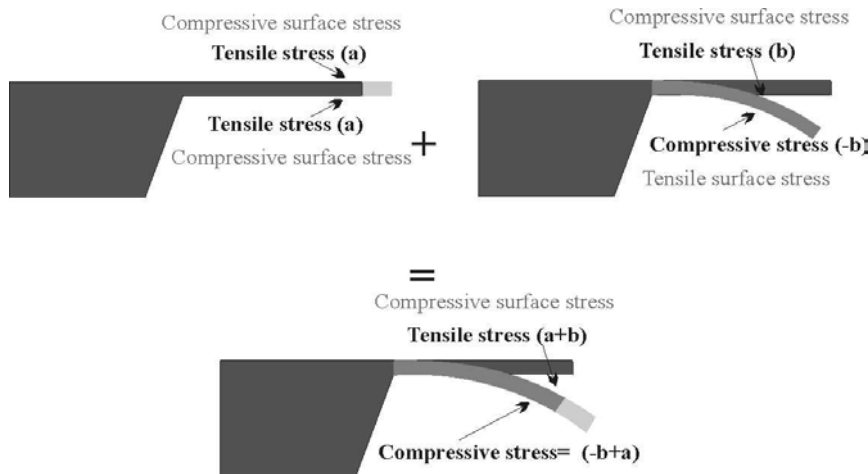


Figure 2.9: The two cantilevers illustrates the two types of stresses acting on the measurement cantilever when exposed to a surface stress on the front side. The front side observes a higher strain than the back side

the resistor on the same side of the neutral axis as the applied surface stress, when a surface stress sensitive cantilever with integrated piezoresistive readout is designed. Thus, obtaining the highest surface strain sensitivity.

2.3.4 Surface-stress on both sides of a simple cantilever

In this section another example of surface stress in a simple cantilever is presented. This time a cantilever consisting of only one layer is exposed to a surface stress σ_s acting on both sides of the cantilever. The resistor thickness equals, in this example, the thickness of the cantilever h . The surface stress sensitivity found from expression

2.3-20 now becomes

$$\left(\frac{\Delta R}{R}\right)_{BS} = -K \left(2\frac{1}{Eh} - \frac{0}{Eh}\right) = -K \left(\frac{2}{Eh}\right) \sigma_s \quad (2.3-23)$$

This result is expected since no bending of the cantilever occurs when the same surface stress is acting on both sides on a simple cantilever. Therefore, the only strain acting is the stretching/compression strain, and the factor 2 is obtained due to the surface stress acting on both sides of the cantilever. The theory also states that the sensitivity is not dependent on the position of the resistor with respect to the neutral axis in the cantilever. This is also expected since the cantilever only experiences a compression/stretching in the lateral direction, and thereby there is no dependency of the neutral axis,

It is seen that the surface stress sensitivity from a simple cantilever with a surface stress acting on one side 2.3-21 is a factor of 2 more sensitive than a simple cantilever exposed to a surface stress on both sides 2.3-23

2.3.5 Bending of a cantilever due to built-in stress

When designing a surface stress sensitive cantilever with integrated piezoresistive read-out, it is usually necessary to build a cantilever consisting of several layers. One layer for defining the resistor, and other layers for encapsulating the resistor and definition of the cantilever. These layers exhibit different build-in stresses. If the differences in the build-in stresses are not considered carefully during the design phase, it is possible to end up with bent cantilevers. An example of such a cantilever is shown in figure 2.10, where the cantilever to the left bend due to a non-optimized build-in stress design, whereas the cantilevers to the right do not bend, because the build-in stress in the layers are taken into account during the design. The surface stress sensitivity of

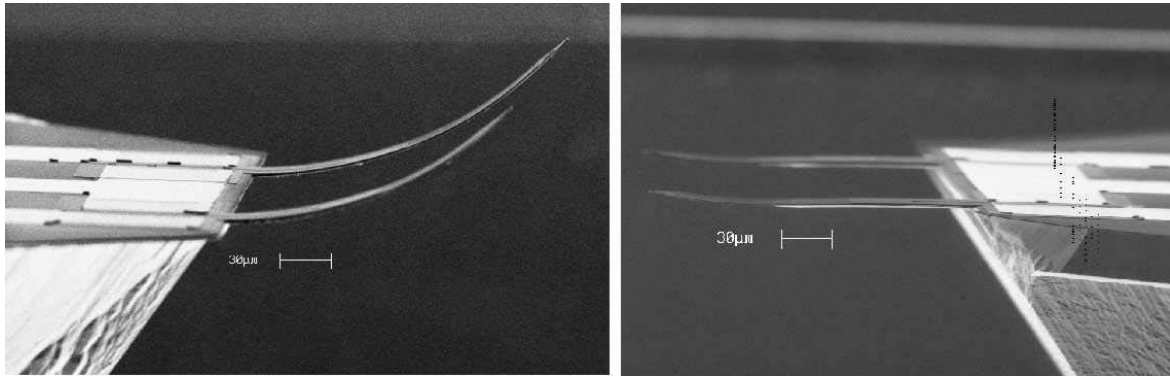


Figure 2.10: *The left cantilever bends due to build-in stress mismatch of the cantilever layer. The right cantilever is straight, because the design took the mismatch into consideration*

a cantilever with a static deflection due to the build-in stress is not altered, since the

different strain effects can be superposed and therefore can be seen as an off-set of the signal. The reason why the bending of the cantilever is still taken into consideration during the design, is that it might be difficult to place a lid on top of a channel in which a very much deflected cantilever is placed.

The bending of the composite cantilever can be determined from the expression for β in expression 2.3-16 in section 2.3.1. The stress σ_i corresponds to the build-in stress in the i th layer. The radius of curvature of the cantilever r equals $\frac{1}{\beta}$, since the cantilever length l at the neutral axis is $l = \theta r$, see figure 2.11 and the cantilever length l_z at the position z with respect to the neutral axis is

$$l_z = l + \Delta l = l(1 + \epsilon(z)) = \theta(r + z) = \theta r(1 + \frac{z}{r}) \quad (2.3-24)$$

From this, the strain can be found to $\epsilon(z) = \frac{z}{r}$ and by comparison with expression 2.3-1, it is seen that $\beta = \frac{1}{r}$. The end deflection y of the cantilever can now be calculated

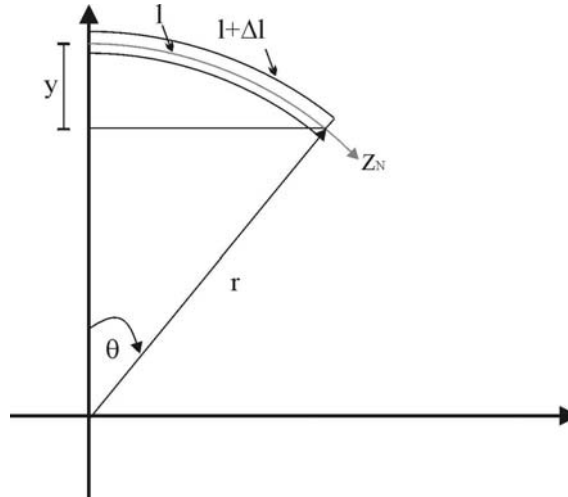


Figure 2.11: From this graph, the radius of curvature r can be found to $\frac{1}{\beta}$. y is the end deflection

since the radius of curvature $r = \frac{1}{\beta}$ is constant. From Phyttagoras, it can be found that $\cos(\theta) = \frac{r-y}{r}$, thus the end deflection becomes

$$y = r(1 - \cos(\theta)) = r(1 - \cos(\frac{l}{r})) = \frac{(1 - \cos(\beta l))}{\beta} \quad (2.3-25)$$

In the case where $y \ll r$, the expression in 2.3-25 can be simplified to

$$y \simeq \frac{1}{2} \frac{l^2}{r} = \frac{1}{2} \beta l^2 \quad (2.3-26)$$

It can be seen from this equation that the end-point deflection of a cantilever with length l due to build-in stress in the cantilever layers, is dependent on β and the square of l . As expected the build-in stresses around the neutral axis have to equal zero in order to obtain a straight cantilever.

2.4 Noise sources in a cantilever with piezoresistive readout

When measuring surface stress changes using a cantilever with integrated piezoresistive readout, the minimum obtainable resolution is governed by the different noise sources that act on the cantilever. In this section, the internal noise sources are discussed, while the external noise sources obtained from the surroundings are not discussed. This is due to the fact that these noise sources are dependent on the place and the time the measurement is performed. An example of an external noise source could be a pump placed next to the measurement setup. Vibrations from the pump might be picked-up in the cantilever resulting in lower resolution. The internal noise sources discussed here are Johnson and Hooge noise, which originate from the piezoresistor, while the vibrational noise is a mechanical noise originating from the thermally induced vibrations in the cantilever.

2.4.1 Vibrational noise

The noise contribution from the thermal vibrations can be found by summing up over all the vibrational modes of the cantilever. In the case of a cantilever used as a surface stress sensitive sensor the frequency of the signal obtained is normally well below the resonant frequency. A filter is therefore used in order to suppress noise from the higher order modes. The noise from a free hanging cantilever is [77]

$$\langle z_v^2 \rangle \approx \frac{k_B T l^2}{27k\lambda(1 - \frac{1}{2}\frac{\lambda}{l})^2} \frac{\Delta f}{f_{res}} \quad (2.4-1)$$

in terms of apparent deflection z_v . T is the temperature, k_B is Boltzmann's constant and Δf is the bandwidth. The $\frac{\Delta f}{f_{res}}$ contribution is an estimate of how large a fraction of the noise is situated in the measurement bandwidth. The estimation is only valid for low quality-factor (Q -factor). In the case of measuring in liquid, the Q -factor is normally very low (<100). As expected, a short and stiff cantilever is less sensitive to thermal vibrations than a long and soft cantilever.

Since the surface stress sensitivity is independent of the cantilever length and width, as derived above, the cantilever should be designed short, and thereby stiff, in order to minimize thermal noise and thereby obtain a high signal-noise ratio.

By inserting 2.4-1 in the expression for the deflection sensitivity 2.2-7, an expression for the noise voltage power is obtained

$$\langle V_v^2 \rangle = K^2 \frac{k_B T z_{NR}^2}{144k\lambda^2 l^2 (1 - \frac{1}{2}\frac{\lambda}{l})} \frac{\Delta f}{f_{res}} V_{sup}^2 \quad (2.4-2)$$

It is seen that the vibrational noise is highly dependent on the resistor and cantilever length.

2.4.2 Johnson noise

Johnson noise or white noise is caused by thermal fluctuations of charge carriers in a resistor. The Johnson noise voltage power $\langle V_J^2 \rangle$ for a resistor with resistance R is given by [78]

$$\langle V_J^2 \rangle = 4k_B T R \Delta f \quad (2.4-3)$$

The Johnson noise depends on the dimensions of the resistor, since $R = \rho \frac{\lambda}{w_R h_R}$, where ρ is the resistivity, w_R is the resistor width, h_R is the thickness of the resistor and λ is the resistor length.

Again, the cantilever should be designed short in order to minimize the noise without influencing the sensitivity. It can also be seen that the resistor should be as wide as possible. The Johnson noise is inversely proportional to the sensitivity with respect to the resistor thickness. Therefore, an optimization of the resistor thickness is necessary in order to obtain the highest signal to noise ratio.

2.4.3 Hooge noise

Hooge noise or 1/f-noise is a frequency dependent noise source in the resistors. A model for the Hooge noise was first described by Hooge *et al.* [79], which states that the 1/f noise voltage power is inversely proportional to the number of carriers N in the resistor. The 1/f noise voltage spectral density, S_{Hf} , is given by

$$S_{Hf} = \frac{\alpha V_{sup}^2}{f N} \quad (2.4-4)$$

where α is a material constant. The noise voltage power in the frequency range from f_{min} to f_{max} is found by integrating the voltage spectral density over the frequency range

$$\langle V_H^2 \rangle = \int_{f_{min}}^{f_{max}} S_{Hf} df = \frac{\alpha V_{sup}^2}{N} \ln \left(\frac{f_{max}}{f_{min}} \right) \quad (2.4-5)$$

This has been used to model the 1/f noise in silicon piezoresistors [77, 80]. α has been shown to have a strong dependency on annealing for single crystalline silicon [81].

The design parameter for the 1/f noise in the piezoresistor is the total number of carriers, which can be written as $N = n \lambda w_R h_R$, where n is the carrier concentration. In order to minimize the noise, the dimensions have to be maximized. This will influence the sensitivity through the resistor thickness. The 1/f noise decreases with resistor length while the Johnson noise increases.

2.4.4 Total noise

The noise from the three noise sources mentioned above can now be added in the following manner

$$\langle V_{tot}^2 \rangle = \langle V_v^2 \rangle + \langle V_J^2 \rangle + \langle V_H^2 \rangle \quad (2.4-6)$$

This expression can now be expressed in terms of an apparent surface stress, by inserting 2.4-6 and 2.3-20 into 2.2-6

$$\langle \sigma_{s,apparent} \rangle = 4 \frac{\sqrt{\langle V_{tot}^2 \rangle}}{V_{sup}} \left(\frac{\Delta R}{R} \right) \cdot \sigma_s^{-1} \quad (2.4-7)$$

The different noise contributions have been plotted as a function of the resistor length

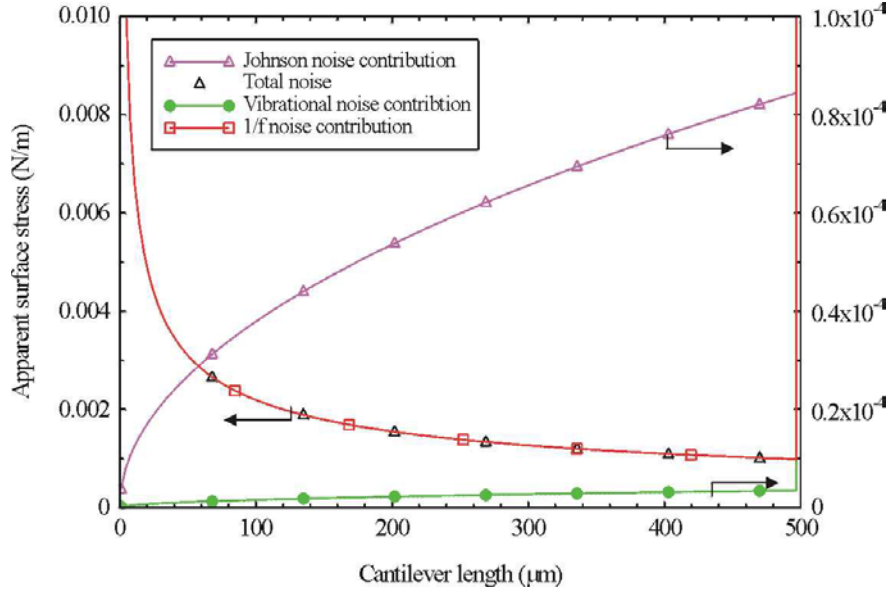


Figure 2.12: The noise expressed in apparent surface stress as a function of resistor/cantilever length. It can be seen that the 1/f noise contribution is by far the largest noise source. Note the two scales on the graph. The cantilever dimensions correspond to design 4 in chapter 4, $\Delta f=50$ Hz and $V_{sup}=4$ V.

λ (in this case: $l=\lambda$) in figure 2.12. As can be seen from the figure the 1/f noise is dominant in the given frequency interval. The vibration noise is seen to be negligible, and this noise source will therefore not be taking into consideration during the optimization for the signal-noise ratio. The Johnson noise increases, as expected, with the resistor length.

2.5 Summary

In this chapter the most important theory concerning surface stress sensitive cantilevers with piezoresistive readout has been discussed. The chapter started out by presenting some basic mechanics which is used to describe the end-point deflection sensitivity for a piezoresistive cantilever. The surface stress sensitivity was derived for a composite cantilever, whereafter two examples simplified the sensitivity expression in order to give an understanding of the important parameters involved. It was found that it is important to place the resistor on the same side of the neutral axis as the applied surface

stress. Finally, the three most important noise sources which determines the minimum detectable surface stress were discussed. It was found that the most important noise source is $1/f$ noise.

Chapter 3

Parameter optimization

This chapter deals with the optimization of the parameters governing the performance of the piezoresistive readout. The optimization is not necessary for a proof-of-principle concept, but is investigated in order to get an idea about the resolution limit for a surface stress sensitive cantilever with piezoresistive readout. First, a characterization of the material constants such as the gauge factor of the piezoresistor and the α -factor in the $1/f$ noise is performed. These two material constants depend on the doping level and the grain size in the silicon. From this characterization, the best material composition can be found and then used for further optimization. Finally, it is possible to perform an optimization of the cantilever dimensions with respect to the signal to noise ratio whereby the minimum detectable surface stress for cantilevers with piezoresistive readout can be found. The signal to noise ratio optimization is performed with respect to the detection of a surface stress change on one side of the cantilever. This result is compared to the minimum detectable surface stress for cantilevers with optical readout.

3.1 Characterization of gauge factors in silicon

From the expression for the surface stress change sensitivity, in equation 2.3-20 and the expression for the deflection sensitivity in equation 2.2-5 it is seen that the sensitivity is proportional to the gauge factor K . It is therefore an advantage to obtain as high a gauge factor as possible in order to maximize the sensitivity.

Silicon exhibits very high gauge factor compared to for example metals. The gauge factor for silicon ranges from 20-170 depending on the grain size and doping of the silicon [82, 75]. The highest gauge factor is obtained from single crystalline silicon. The gauge factor for metals is only on the order of 2 [83]. Therefore, silicon piezoresistors are often used as transducers in micromechanical components. In silicon, the piezoresistive behavior is in principle caused by a change in the band structure, when the crystal is strained. This change is highly anisotropic so that the charge carrier mobility is different in the different crystal directions [83].

The literature does not describe the change in gauge factor as function of the grain sizes in polysilicon. Therefore a characterization of the gauge factor's dependency on doping and annealing as a function of polysilicon grain size and single crystalline silicon is presented in the following.

Cantilevers with integrated piezoresistive readout were fabricated by use of the masks and the fabrications sequence described in chapter 6. During the fabrication, the resistor material was changed. For fabrication of polysilicon resistors a low pressure chemical vapor deposition (LPCVD) technique was used. The temperature in the deposition was changed in order to obtain different grain sizes. The two deposition temperatures used were 580 °C and 620 °C, resulted in amorphous silicon and microcrystalline silicon respectively. For the fabrication of single crystalline silicon resistors, a silicon on insulator (SOI) wafer was used with an oxide layer of 400 nm and a silicon layer of 150 nm. Figure 3.1 shows a cross-sectional schematic of the fabricated cantilevers. It can

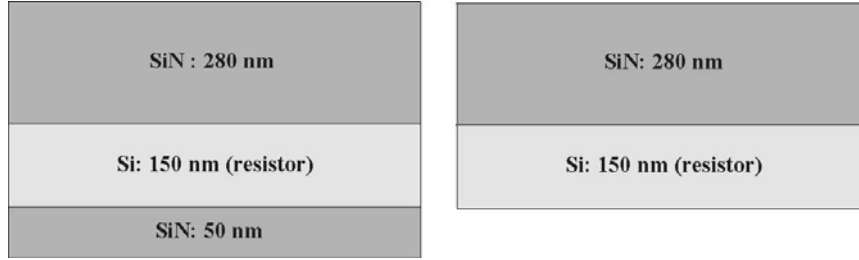


Figure 3.1: Cross-section of the cantilever for the gauge factor characterization. The right cantilever (with single crystalline silicon resistors) lacks the lower nitride layer due to the use of a SOI wafer in the fabrication.

be seen from the figure that the cantilevers with single crystalline silicon resistors did not have a silicon nitride layer on the backside. This difference in cantilever design was due to the use of SOI wafers for the fabrication of single crystalline silicon resistors instead of normal wafers for the fabrication of polysilicon resistors.

The gauge factor of the piezoresistors is determined by measuring the resistance change when forcing, in a controlled way, the cantilever to deflect. This was performed in a setup where a thin needle, controlled by a micro-manipulator, is placed at the apex of the cantilever. The micro-manipulator can then move the needle in the z-direction in steps of 5 μm , thereby deflecting the cantilever downwards. Figure 3.2 shows how the needle presses down on one of the two cantilevers. Note the change in reflection when the cantilever is bent. The change in resistance is simultaneously measured and the result can be plotted as the relative change in resistance ($\frac{\Delta R}{R}$) as a function of the deflection. An example of such a plot can be seen in figure 3.3. The slope in the plot defines the deflection sensitivity for the piezoresistive cantilever. By inserting the sensitivity, the cantilever dimensions and the material parameters in the expression for the deflection sensitivity, equation 2.2-5, the gauge factor can be found.

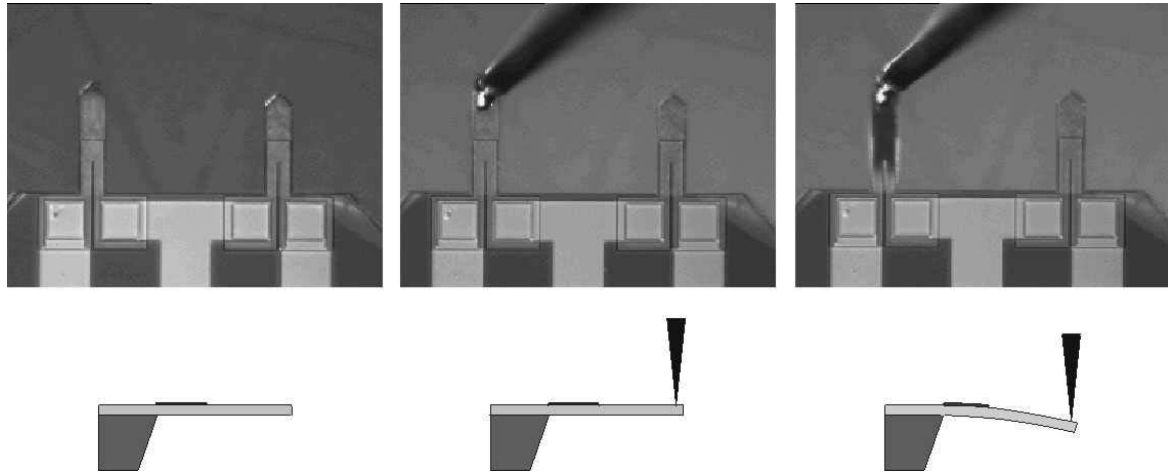


Figure 3.2: The cantilever deflection principle. The upper part shows a top view of the actual deflection of the cantilevers when deflected by the needle. The lower part shows a schematic side view of the principle.

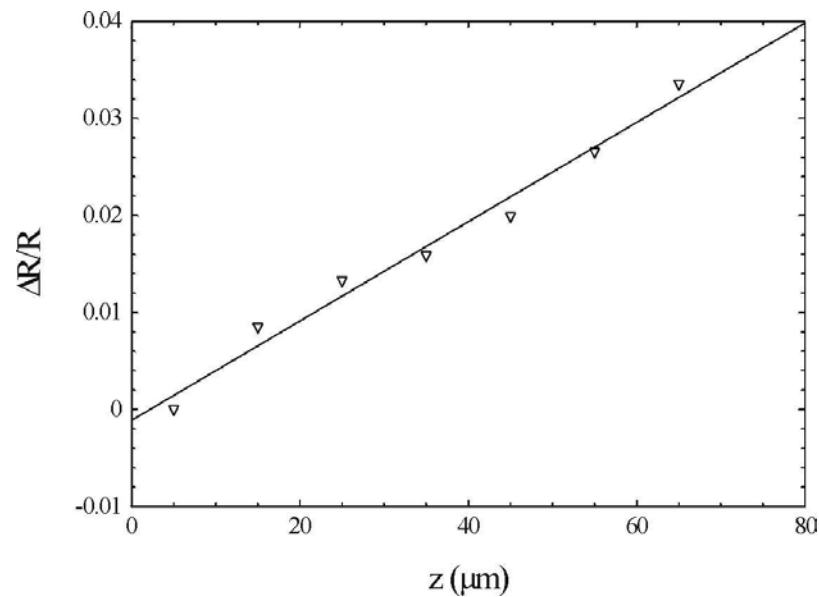


Figure 3.3: The graph shows as plot of relative change in resistance as a function of deflection. The measurement points are marked by triangles and a line is fitted to the data points. The deflection sensitivity can be found from the slope of the fitted line.

The results for the measured gauge factors are listed in table 3.1. The cantilevers with single crystalline silicon have been doped with a boron concentration level of $3 \cdot 10^{-19} \text{ cm}^{-3}$ and $3 \cdot 10^{-20} \text{ cm}^{-3}$. The piezoresistors have then been annealed at 950°C and 1050°C . From the table it can be seen that the low doped highly annealed resistors exhibits the highest gauge factor. This is also in agreement with the literature [84]. The gauge factor for polysilicon is very dependent on the doping and less dependent

Materials	Annealing at 950 °C in 10 min			Annealing at 1050 °C in 30 min		
	Doping level (cm ⁻³)			Doping level (cm ⁻³)		
	3 · 10 ¹⁸	3 · 10 ¹⁹	3 · 10 ²⁰	3 · 10 ¹⁸	3 · 10 ¹⁹	3 · 10 ²⁰
Amorphous silicon	—	31	22	—	32	19
Microcrystalline silicon	—	35	22	—	36	27
Single crystalline silicon	90	50	—	95	55	—

Table 3.1: Measurements of the gauge factor. It is seen that the gauge factors are highly dependent on the doping level, whereas the gauge factor is more or less independent on the annealing conditions.

on the annealing. The gauge factor decreases by up to about 40 % when the doping is increased.

The cantilevers with the polysilicon resistors (amorphous and microcrystalline silicon) have been doped with a boron doping concentration level of about a factor of 10 times higher than the single crystalline silicon resistors. This is due to the fact that single crystalline silicon is a 10 times better electrical conductor than polysilicon [84]. The polysilicon silicon resistors have been annealed at the same temperature and time as the single crystalline resistors. The table shows that the highest gauge factor is obtained for low doped microcrystalline silicon. Furthermore, the table shows that the gauge factors are not that dependent on the annealing, but very dependent on the doping level. Again, the gauge factor decreases by up to 40 % when the doping is increased.

3.2 Characterization of 1/f noise in silicon piezoresistors

1/f-noise is the main contribution to the noise at low frequencies. Since the measured surface stress change is normally obtained with sampling rates in the order of 10th of milliseconds, the measurement bandwidth is normally limited with a low-pass filter to about 20-100 Hz. The minimum detectable surface stress is therefore very dependent on the 1/f-noise. In the expression for the 1/f-noise in equation 2.4-5, α which is a material parameter and N which is the total number of carriers are the two parameters which can be optimized.

In order to optimize N and α , silicon resistors inserted in Wheatstone bridges have been fabricated. The resistors have been fabricated with different dimensions, silicon grain size, doping levels and annealing time. The Wheatstone bridges are fabricated using standard microfabrication technology.

3.2.1 Fabrication of resistors for 1/f-noise characterization

500 μm thick silicon wafers were used for the fabrication of the polysilicon resistors. These were oxidized in order to grow a 300 nm thick silicon oxide, see figure 3.4a. Hereafter a 150 nm thick polysilicon layer was deposited using LPCVD. The polysilicon

Material	Temp.($^{\circ}\text{C}$)	Doping level (cm^{-3})	Annealing ($^{\circ}\text{C}$)
Amorphous	580	$3 \cdot 10^{19} / 3 \cdot 10^{20}$	950 / 1050
Microcrys.	620	$3 \cdot 10^{19} / 3 \cdot 10^{20}$	950 / 1050
Single crys.		$3 \cdot 10^{18} / 3 \cdot 10^{19}$	950 / 1050

Table 3.2: Resistor material parameter. For each chip design there have been fabricated chips with low annealing (950°C) and high annealing (1050°C) and also with two different doping level.

was again deposited at 580°C and 620°C corresponding to amorphous- and micro-crystalline silicon (3.4b). At this point, SOI wafers for the fabrication of the single crystalline silicon resistors were included in the fabrication process. The buried silicon oxide is 300 nm thick, and the silicon top layer 150 nm thick. The wafers were then boron implanted at the doses given in table 3.2. Next, the mask defining the resistor was transferred to the wafers using photolithography and the wafers were etched using reactive ion etching (RIE)(3.4c). A thin thermal silicon oxide was grown on top of the resistors for the encapsulation and the wafers were annealed at the temperatures given in table 3.2 (3.4d). Contact holes were etched in the silicon oxide for the electrical contacts (3.4e) and finally metal was deposited for the electrical contacts.

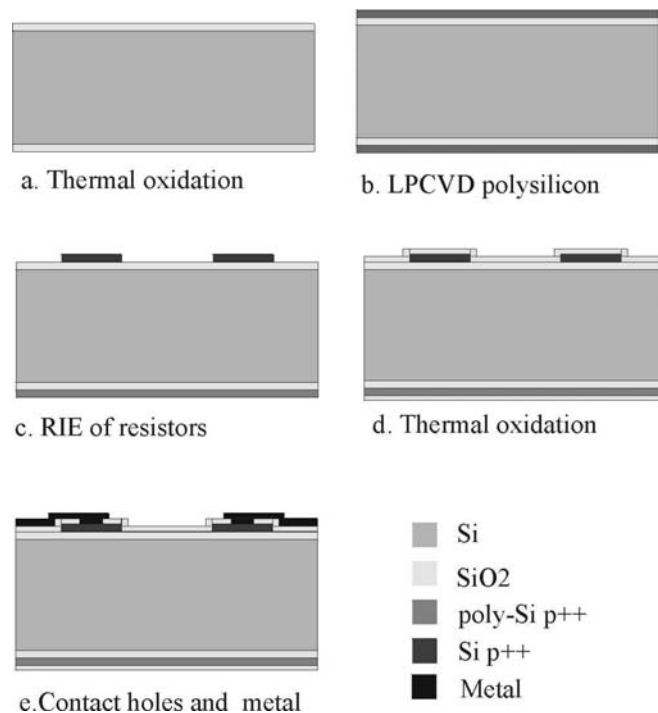


Figure 3.4: The fabrication process for the resistors used for characterization of 1/f noise in silicon piezoresistors.

Figure 3.5 shows the chip layout for the resistors. It can be seen from the figure that a chip consists of 16 different Wheatstone bridge configurations. The dimensions of the

l/w	Resistor width $w(\mu m)$			
	5	10	15	20
5	25	50	100	200
10	50	100	200	400
20	100	200	400	800

Table 3.3: The length of the resistor is given as a function of the width and the ratio between the length and width is shown.

resistors on the chip are given in table 3.3. The resistors are designed with an *I*-shape. Figure 3.6 shows an image of a finished Wheatstone bridge.

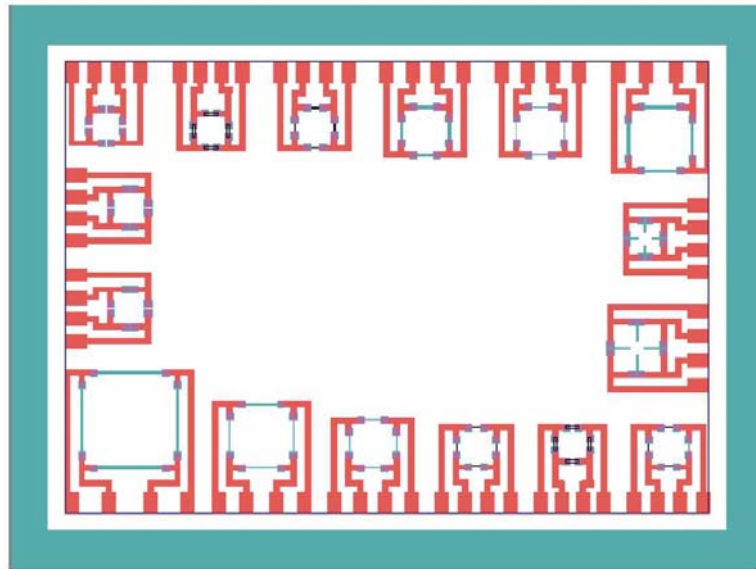


Figure 3.5: Chip layout for the resistors. The resistor designs are *I*-shaped with different dimensions. There are 16 Wheatstone bridge configurations per chip.

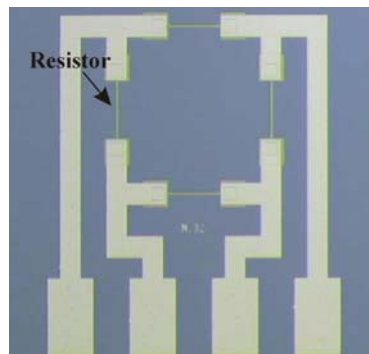


Figure 3.6: Optical microscope image of a fabricated Wheatstone bridge.

3.2.2 Characterization of 1/f-noise

The 1/f-noise of the silicon resistors in the Wheatstone bridge configurations is measured using the setup shown in figure 3.7. The noise in the Wheatstone bridge is measured using a spectrum analyzer, which can measure voltage noise as a function of the frequency. For each resistor design and material composition the noise is measured as a function of the supply voltage. A filter and a pre-amplification step are inserted between the Wheatstone bridge and the spectrum analyzer in order to remove the DC-voltage contribution and to obtain signals higher than the noise floor of the spectrum analyzer respectively.

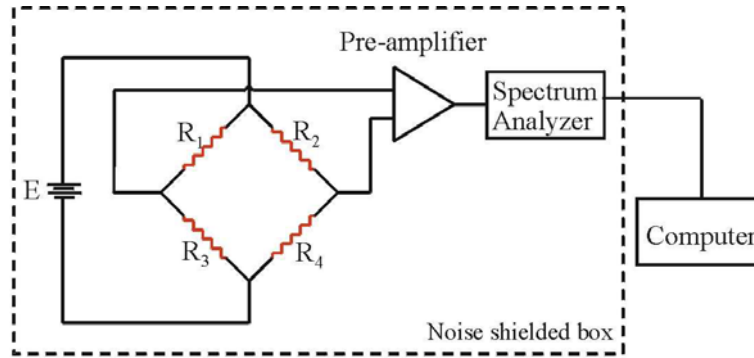


Figure 3.7: Schematic of the noise measurement circuit. The noise in the different Wheatstone bridge configurations is measured as a function of the supply voltage by means of a spectrum analyzer.

An example of an 1/f-noise measurement is given in figure 3.8. The voltage noise spectral density is plotted as a function of the frequency. Figure shows 5 noise curves each corresponding to one supply voltage. It can be seen that the 1/f noise is very dependent on the supply voltage, which is also expected from the 1/f noise theory. It can also be seen from the graph that the noise floor, the Johnson noise, increases slightly as a function of the supply voltage. From the Johnson noise theory, it is not expected that the noise increases as a function of the supply voltage. The reason for the increase is probably due to the self heating of the resistors, since Johnson noise is a function of the temperature in the resistor. From figure 3.8 it can be seen that the difference in noise floors due to a change in supply voltage from $V_{sup}=0$ V to $V_{sup}=9$ V is about a factor of 1.3. This equals a temperature increase of approximately 200 °C. This temperature increase seems realistic.

3.2.3 Data discussion

A large amount of data has been obtained during the 1/f noise measurements. 16 different silicon resistor material compositions have been fabricated, see table 3.2 with each 16 different resistor designs, see table 3.3. From these data it has been possible to

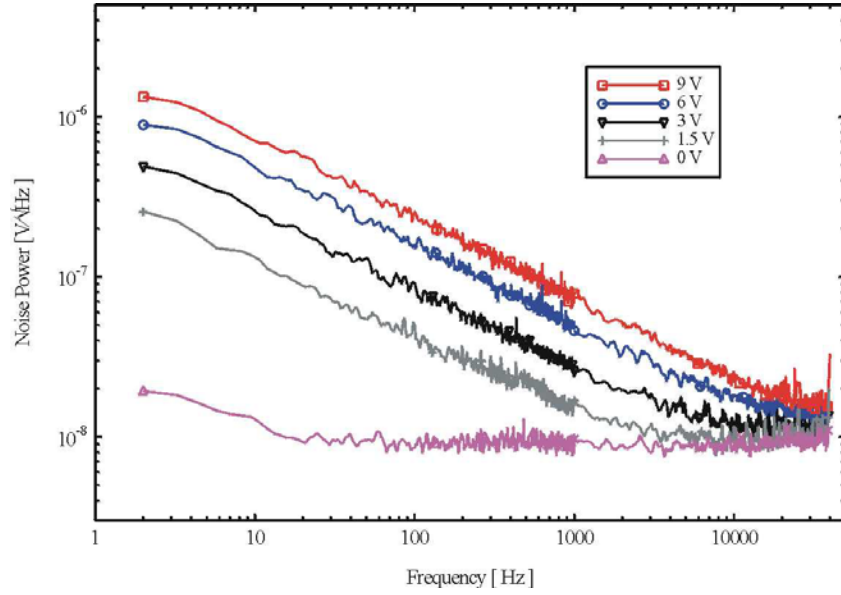


Figure 3.8: The graph shows a plot of a noise measurement result. The result is plotted as the voltage noise as a function of the frequency. It can be seen from the plots that the 1/f noise is very dependent on the supply voltage.

obtain relations between the material parameter, the design and the 1/f noise. From the expression for the 1/f-noise in equation 2.4-4

$$S_{Hf} = \frac{\alpha V_{sup}^2}{fN}$$

it can be seen that the 1/f-noise is very dependent on the total number of carriers, which can be written as $N = n l w h$, where n is the doping concentration, l is the resistor length, w is the resistor width and h is the resistor thickness. Inserting this in the expression for the 1/f-noise (2.4-4), it can be seen that the noise is dependent on the volume of the resistor. This is in good agreement with the obtained results. In figure 3.9 the voltage noise is plotted as a function of the frequency. The plots show graphs where the $l/w = 5$ is kept constant while the resistor length is changed. It can be seen that the noise increases when the volume is decreased, as expected from the theory.

The results from the 1/f noise measurements presented so far are in good agreement with the Hooge expression for the 1/f noise 2.4-4. The figures have shown that the 1/f noise is dependent on the supply voltage and the resistor dimensions. But the reason for the change in 1/f noise with respect to for example annealing is not explained directly in the expression.

An example of the effect of the annealing temperature and annealing time is shown in figure 3.10. The noise measurements for two Wheatstone bridges with microcrystalline

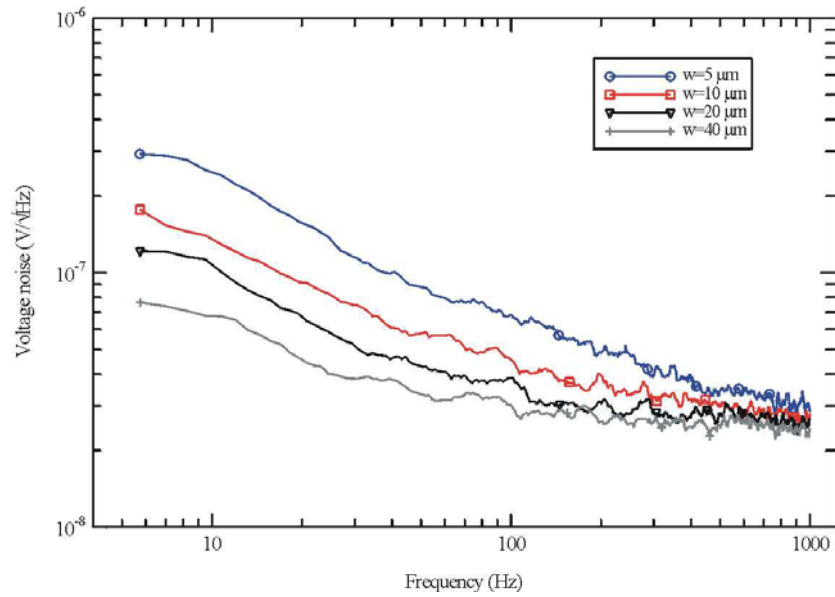


Figure 3.9: The graph shows the 1/f noise measurements for single crystalline silicon with a doping concentration of $n = 3 \cdot 10^{18} \text{ cm}^{-3}$ and $l/w = 5$. The plot shows that the noise decreases as the resistor volume increases.

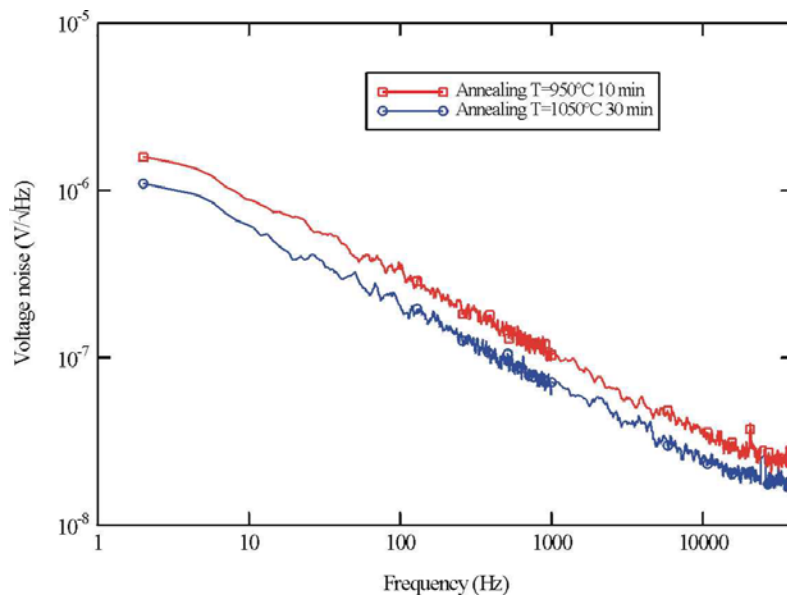


Figure 3.10: The graphs shows the measurements for two Wheatstone bridges with microcrystalline silicon resistors annealed differently. It can be seen that annealing at the high temperature, reduces the 1/f-noise level a factor of 1.5.

silicon resistors annealed differently are shown. The resistors have the same size and same doping concentration. It is seen from the graph that the 1050 °C in 30 minutes annealing treatment reduces the 1/f-noise level approximately a factor of 1.5 compared

to the 1/f noise level for an annealing at 950 °C in 10 min.

The effect of the annealing and also the silicon material composition e.g. microcrystalline or single crystalline silicon, are incorporated in the α -factor. The α factor can therefore be considered to be a material constant. In order to obtain the lowest 1/f noise in the piezoresistor, it is important to choose the resistor material with respect to the α -factor. The α -factor can be found from the 1/f noise graphs by using the following reformulation of the Hooge expression 2.4-4. The total number of carriers can be written as a function of the w/l -ratio

$$N = N_D w l = N_D l^2 (l/w)^{-1} \quad (3.2-2)$$

where $N_D = n \cdot h$. Inserting this in the equation for the 1/f-noise expression 2.4-4 yields

$$\sqrt{S_{Hf} f} = \sqrt{\frac{\alpha V_{sup}^2 (l/w)}{N_D}} \frac{1}{l} \quad (3.2-3)$$

When the supply voltage, doping dose and the w/l -ratio are kept constant, $\sqrt{S_{Hf} f}$ can be plotted as a function of $\frac{1}{l}$ for each silicon material composition. A linear relation can be found from which the α -factor can be determined from the slope. An example of such a plot is given in figure 3.11. The plot shows the linear relation for amorphous- and microcrystalline silicon. The doping level is $N_D = 5 \cdot 10^{15} \text{ cm}^{-2}$, $V_{sup} = 6 \text{ V}$ and $(l/w) = 5$. The lower the slope, the lower the α -factor.

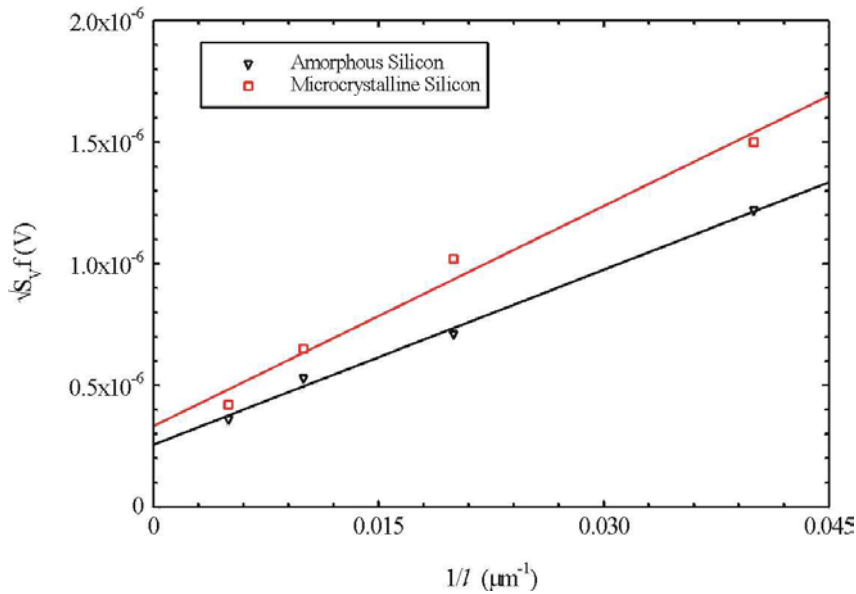


Figure 3.11: The plot shows the linear relationship between $\sqrt{S_{Hf} f}$ and $\frac{1}{l}$ for amorphous- and microcrystalline silicon. $N_D = 5 \cdot 10^{15} \text{ cm}^{-2}$, $V_{sup} = 6 \text{ V}$ and $(l/w) = 5$.

In the Hooge expression for the 1/f noise power, the 1/f noise power is inversely proportional to the total number of carriers and thereby the doping concentration. This means that an increase by a factor 10 in doping concentration will decrease the 1/f noise with a factor of $\sqrt{10}$ in the voltage noise. The doping concentration dependency is seen in figure 3.12, where the $\sqrt{S_{Hff}}$ is plotted as a function of $\frac{1}{l}$ for microcrystalline silicon. The difference in the noise level for the two doping level concentrations is determined by the slopes. In index numbers, the slope for a doping level concentration of $N_D = 5 \cdot 10^{14} \text{ cm}^{-2}$ is defined to $a_{low} = 1$ and the slope for a doping concentration of $N_D = 5 \cdot 10^{15} \text{ cm}^{-2}$ is measured to $a_{high} = 3.1$. As expected from the theory, the difference in the noise level due to the doping concentration is close to $\sqrt{10}$.

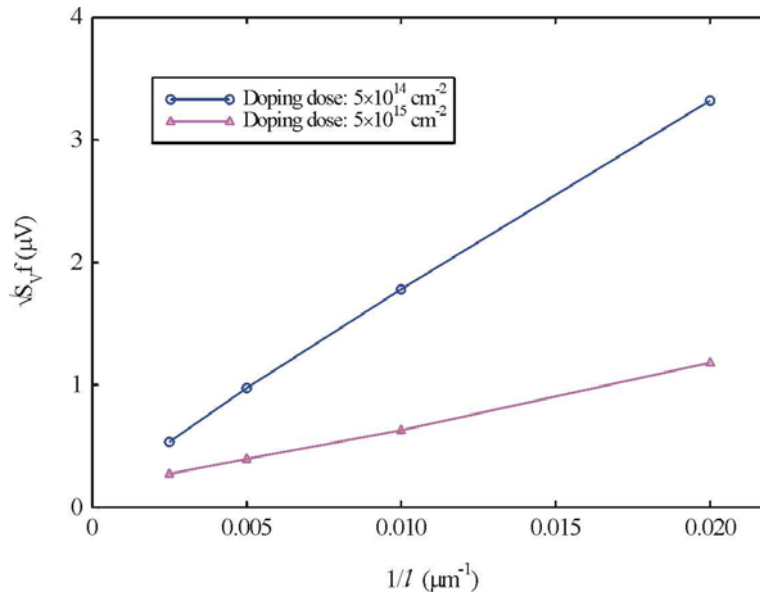


Figure 3.12: The graphs shows that the doping concentration for low doped microcrystalline silicon. The doping doses are: $N_D = 5 \cdot 10^{14}$ and $N_D = 5 \cdot 10^{15}$ for the high and the low doped silicon respectively. It is seen that the doping dose has a high influence on the 1/f noise level. The noise level is reduced a factor of 3.1 when increasing the doping concentration a factor of 10.

It is now possible to produce graphs as the ones presented in figure 3.11 and 3.12 and thereby determine the α -factors as a function of the material parameters. This has been performed and the results are listed in table 3.4. The results show that the α -factor for the single crystalline silicon material is more than two orders of magnitude lower than the α -factor for polysilicon. It is seen from the single crystalline silicon results, that the α -factor depends strongly on the annealing temperature, but only slightly on the doping dose. The dependency on annealing time corresponds very well with J.Harley *et al.* [85] who also reports on decreasing α -factors as a function of increasing annealing time. The same dependency is observed for the polysilicon material, but the dependency is not so pronounced as for single crystalline silicon. The lowest α -factor

Materials	Annealing at 950 °C in 10 min			Annealing at 1050 °C in 30 min		
	Doping dose (cm ⁻²)			Doping dose (cm ⁻²)		
	5 · 10 ¹³	5 · 10 ¹⁴	5 · 10 ¹⁵	5 · 10 ¹³	5 · 10 ¹⁴	5 · 10 ¹⁵
Amorphous silicon	—	1.3 · 10 ⁻³	1.3 · 10 ⁻³	—	6.5 · 10 ⁻⁴	8.0 · 10 ⁻⁴
Microcrystalline silicon	—	1.8 · 10 ⁻³	1.5 · 10 ⁻³	—	9.9 · 10 ⁻⁴	1.4 · 10 ⁻³
Single crystalline silicon	5.0 · 10 ⁻⁶	5.7 · 10 ⁻⁶	—	3.2 · 10 ⁻⁶	3.2 · 10 ⁻⁶	—

Table 3.4: The table shows the measured α -factors. It can be seen that the smallest α -factor is found in high annealed single crystalline silicon.

for the single crystalline silicon is measured to $\alpha_{min} = 3.2 \cdot 10^{-6}$ at high annealing conditions. For the polysilicon materials, the lowest α -factor is found for low doped, highly annealed amorphous silicon to $\alpha_{min,amorph} = 6.5 \cdot 10^{-4}$. The measurements do not show any significant difference in 1/f-noise as a function of the l/w -ratio for constant resistor dimensions, thus the α -factor is a material constant.

3.3 Signal to noise optimization

This section deals with the optimization of the parameters. The resistor design, resistor dimensions, silicon material and supply voltage are optimized for the highest signal to noise ratio and thereby the minimum detectable surface stress obtainable with a surface stress sensitive cantilever with piezoresistive readout. From the gauge factor characterization and the α -factor characterization it is seen that the highest gauge factor and the lowest α -factor are not obtained for the same material parameters, with exception of single crystalline silicon. In the first part of this section the signal to noise ratio for the different silicon materials is calculated in order to decide what type of silicon materials should be used for the piezoresistor material. This result is then used for optimizing the rest of the parameters.

3.3.1 Calculation of the signal to noise ratio in the different silicon materials

The signal to noise ratio with respect to the material parameters can be determined by keeping the resistor and cantilever dimensions constant and then only changing the gauge factor, doping dose, annealing time and α -factor as a function of the material. The resistivity can in principle be calculated when the doping dose and the silicon material is known. But since the grain size and the number of activated electrical carriers depend on the annealing time and temperature, the actual resistance is instead measured. In table 3.5, the resistance of resistors with a length of $l = 100 \mu m$ a width of $w = 36 \mu m$ and a thickness of $h = 150 \text{ nm}$ are listed as a function of material composition. As expected, the highly doped resistors exhibit lower resistivity. Theoretically, it would be expected that the resistivity is a linear function of the doping dose. The reason why this is not true is probably due to the fact that less than 100 % of the boron ions are activated and the actual resistance therefore also becomes highly dependent on the annealing temperature.

Materials	Annealing at 950 ^o C in 10 min			Annealing at 1050 ^o C in 30 min		
	Doping dose (cm ⁻²)			Doping dose (cm ⁻²)		
	5 · 10 ¹³	5 · 10 ¹⁴	5 · 10 ¹⁵	5 · 10 ¹³	5 · 10 ¹⁴	5 · 10 ¹⁵
Amorphous silicon	—	13.5 kΩ	2.9 kΩ	—	13.9 kΩ	2.1 kΩ
Microcrystalline silicon	—	75.0 kΩ	4.3 kΩ	—	25.4 kΩ	2.6 kΩ
Single crystalline silicon	21.5 kΩ	4.2 kΩ	—	25 kΩ	3.0 kΩ	—

Table 3.5: The table shows the measured resistor values, for a resistor with a length of $l = 100 \mu m$, a width of $w = 36 \mu m$ and a thickness of $h = 150 nm$.

Materials	Annealing at 950 ^o C in 10 min			Annealing at 1050 ^o C in 30 min		
	Doping dose (cm ⁻²)			Doping dose (cm ⁻²)		
	5 · 10 ¹³	5 · 10 ¹⁴	5 · 10 ¹⁵	5 · 10 ¹³	5 · 10 ¹⁴	5 · 10 ¹⁵
Amorphous silicon	—	1.1	1.9	—	1.5	2.6
Microcrystalline silicon	—	1.0	2.2	—	1.4	2.8
Single crystalline silicon	13.4	21.0	—	16.7	29.6	—

Table 3.6: The table shows the calculated values for the signal to noise ratio with respect to material parameters. The signal to noise ratio is given as an index number with respect to low doped low annealed microcrystalline silicon.

The signal to noise ratio can be written as

$$S/N = \frac{(\frac{1}{4} \frac{\Delta R}{R}) / \sigma_s V_{sup}}{\sqrt{S_H + S_J}} \quad (3.3-1)$$

where the surface stress sensitivity is given by equation 2.3-20, the 1/f noise in voltage power S_H in equation 2.4-5 and the Johnson noise S_J in equation 2.4-3. The signal to noise ratio is now found by using the resistor dimensions and values given in table 3.5 and keeping the cantilever dimensions constant. Note that the supply voltage in the expression for the 1/f-noise is half the supply voltage in the expression for the surface stress sensitivity, due to the fact that the resistor is inserted in a Wheatstone bridge and the voltage drop over the measurement resistor is only half the voltage drop over the whole bridge. The signal to noise ratio is given in table 3.6. In the table the signal to noise ratio is given as an index number, where the signal to noise ratio for low doped low annealed microcrystalline silicon has index 1.0. The supply voltage used is $V_{sup} = 5 V$ and the bandwidth is $\Delta f = 50 Hz$ ($f_{min} = 1 Hz$ to $f_{max} = 51 Hz$).

It is seen that a high doping level and a high temperature annealing give the highest signal to noise ratio. The result is not expected if only the gauge factors only were taken into account, since the highest gauge factors are obtained for lower doping doses. The highest signal to noise ratio is obtained from single crystalline silicon, as expected. For the polysilicon material, the microcrystalline silicon exhibits the highest signal to noise ratio. This result indicates that the larger the grain size the better the signal to noise ratio becomes.

From the gauge factor and 1/f-noise characterization and the signal to noise ratio

with respect to these two parameters, it can be concluded that highly doped, high temperature annealed single crystalline silicon has the highest signal to noise ratio, which is about a factor of 10 times better than highly doped, high temperature annealed microcrystalline silicon.

3.3.2 Signal to noise ratio with respect to cantilever dimensions

The optimization of the signal to noise ratio with respect to the cantilever dimensions is much more difficult to perform than the optimization of the signal to noise ratio with respect to the material parameters. This is due to the fact that more parameters are involved in this optimization. In order to get an idea of what the most sensitive cantilever design is, the most important parameters will be discussed in the following.

For optimizing the single sided surface stress change sensitivity, the expression in 2.3-20 is once again considered

$$\frac{\Delta R}{R} = K \left(-\frac{1}{\sum_i E_i h_i} - \frac{z_T(z_T - \sum_{j=0}^R h_j + \frac{h_R}{2})}{\sum_i E_i h_i ((z_T - \sum_{j=0}^i h_j + \frac{h_i}{2})^2 + \frac{1}{3}(\frac{h_i}{2})^2)} \right) \sigma_s$$

From the expression it is seen, that the thickness of the cantilever, h and the Young's modulus E of the individual layers, have to be minimized, while the distance between the resistor and the neutral axis has to be maximized. As stated before it is also important that the resistor is placed on the same side of the neutral axis as the applied surface stress. The resistor has to be completely encapsulated in a material which is a very good diffusion barrier with respect to water and sodium, due to the fact that the cantilevers are used for measurements in liquid environments. Silicon nitride has shown to serve as a good diffusion barrier [84] in contrast to silicon oxide, which is a very poor diffusion barrier. Silicon nitride is therefore chosen to define the cantilever and the encapsulation of the resistors. The silicon nitride used, is a so-called silicon rich nitride, which exhibits low build-in stress ($\sigma \simeq 50 \text{ MPa}$) [86], and a Young's modulus of $E = 250 \text{ GPa}$.

In order to place the resistor as far away from the neutral axis as possible, the resistor should in principle be infinitely thin and the cantilever very thick and stiff. This contradicts the requirement of a thin and soft cantilever in the surface stress sensitivity expression, and an optimization is required. The two noise contributions are expressed again

$$\begin{aligned} \langle V_H^2 \rangle &= \int_{f_{min}}^{f_{max}} S_H f df = \frac{\alpha V_{sup}^2}{N} \ln\left(\frac{f_{max}}{f_{min}}\right) \\ \langle V_J^2 \rangle &= 4k_B T R \Delta f \end{aligned}$$

where $\langle V_H^2 \rangle$ is the $1/f$ noise power and $\langle V_J^2 \rangle$ is the Johnson noise power. Since $R = \rho \frac{\lambda}{w_R h_R}$ and $N = n \lambda w_R h_R$ it is seen that the noise increases with decreasing resistor thickness. From these expressions it is also seen that the $1/f$ noise decreases when

the resistor is long and wide, while the Johnson noise decreases when the cantilever length decreases and the width increases. Since the total noise decreases as a function of increasing resistor width, and the surface stress sensitivity is independent on the cantilever width, no optimization is needed for the cantilever and the resistor width. It is determined by the maximum allowable cantilever width in the design. The resistor length and thereby the cantilever length, has to be optimized in order to decrease the total noise, and the resistor thickness has to be optimized in order to optimize the signal to noise ratio.

The optimization of the parameters has been performed by using a small program in Maple [87], using the expressions for the signal to noise ratio, given in expression 3.3-1. Since the noise is dependent on the used bandwidth, the optimization was done for $\Delta f = 1 \text{ Hz} - 51 \text{ Hz}$. Table 3.7 shows the results of the optimization. The table shows the optimization for both single crystalline silicon resistors and microcrystalline silicon resistors. As expected, the lowest detectable surface stress is found for the single crystalline silicon. By comparison with the microcrystalline silicon it is seen that the single crystalline silicon is a factor of a 10 better.

The supply voltage has also been optimized since both the sensitivity and the $1/f$ noise increases a function of the supply voltage. A maximum of $V_{sup} = 5 \text{ V}$ is allowed in order not to apply too much power to the resistors, figure 3.13 show the signal to noise ratio as a function of supply voltage V_{sup} . It can be seen in figure 3.13 that signal to noise ratios very close to the optimum, is obtained for supply voltages higher than $V_{sup} = 2 \text{ V}$.

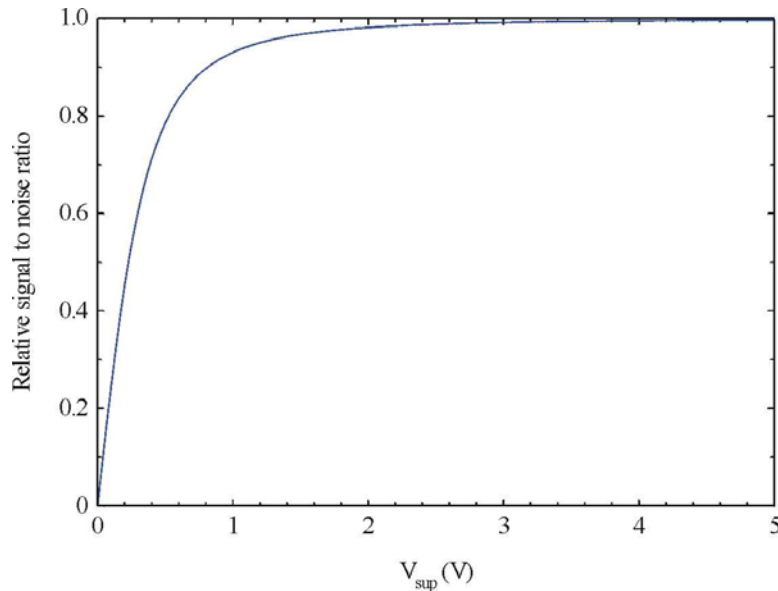


Figure 3.13: Signal to noise ratio optimization as a function of supply voltage for $\Delta f = 1 - 51 \text{ Hz}$.

Δf [Hz]	λ [μm]	$\frac{\Delta R}{R}/\sigma_s$ [m/N]	$\sigma_{s,min}$ [N/m]	k [N/m]	f_{res} [kHz]	$\frac{\Delta R}{R}/z$ [nm ⁻¹]
Microcrystalline 1-51	1267	$-7.1 \cdot 10^{-4}$	$2.6 \cdot 10^{-4}$	$1.9 \cdot 10^{-4}$	0.29	$0.35 \cdot 10^{-6}$
Single crystalline 1-51	198	$-1.3 \cdot 10^{-3}$	$5.7 \cdot 10^{-5}$	0.030	8.6	$0.13 \cdot 10^{-6}$

Table 3.7: The table shows the surface stress sensitivity, resolution and the mechanical parameters as a function of optimized cantilever dimensions. The metal layer and the upper silicon nitride layer is given to 40 nm and 50 nm respectively. The optimized resistor thickness was found to $h_{res,opt} = 160$ nm, and the lower silicon nitride layer was optimized to $h_{low,nitr} = 205$ nm. The cantilever length is defined to $l = \lambda + 44 \mu m$. The cantilever width is set to $w = 90 \mu m$.

3.3.3 Minimum detectable surface stress in a cantilever with optical readout

The optical readout system is the most commonly used readout system in AFM. As described previously, this system is very sensitive when measuring cantilever deflections. In this section the piezoresistive readout system is compared to the optical readout system.

The noise sources in the optical readout system is determined by shot noise in the photo detector, Johnson noise and 1/f noise in the electrical circuit [88]. These noise sources are very dependent on the actual readout system, and is therefore not considered here. In practice, the most important noise source is the random thermal vibrations in the cantilever. The minimum detectable deflection z_{min} can be expressed as [89]

$$z_{min} = \sqrt{\frac{4k_B T \Delta f}{2\pi Q k f_{res}}} \quad (3.3-3)$$

where Q is the quality factor. The surface stress sensitivity can be found from Stoney's formular [90]

$$\sigma_s = \frac{1}{R} \frac{E h^2}{6} \quad (3.3-4)$$

inserting the expression for the radius of curvature R from expression 2.3-26 into Stoney's formular 3.3-4 and using the expression for the spring constant 2.1-2 and the resonant frequency 2.1-5, the expression for the minimum detectable surface stress in a cantilever with optical readout is given by

$$\sigma_{s,min} = \frac{4}{3} \sqrt{\frac{k_B T \Delta f \rho^{1/2} E^{1/2} l}{Q}} \frac{l}{w}; \quad (3.3-5)$$

where ρ is the mass density of the cantilever material. Surprisingly, the minimum detectable surface stress, with respect to thermal vibrations is not dependent on the cantilever thickness h . This is because the end-point vibration is inversely proportional

with the cantilever thickness. Nevertheless, a cantilever with optical readout has to be designed reasonably thin, since the noise sources in the readout system mentioned above will be dominant for very small end-point deflections.

The expression for the minimum detectable surface stress also shows that the cantilever material parameters, E and ρ have very little influence on the performance. The most important parameter is the l/w relation which should be minimized in order to maximize the resolution. In practice, the relation will be about 1.

A silicon cantilever with $l/w = 1$ and a quality factor of $Q = 1$ which is normally obtained in liquid is given as an example. Using $E = 180 \text{ GPa}$, $\rho = 2330 \text{ kg} \cdot \text{m}^{-3}$, $\Delta f = 50 \text{ Hz}$ and $T = 300 \text{ K}$, the minimum detectable surface stress is found to $\sigma_{s,min} \simeq 5 \cdot 10^{-6} \text{ N/m}$. By comparison with the minimum detectable surface stress for a cantilever with piezoresistive readout it is seen that the optical readout is a factor of 10 more sensitive. This difference in resolution is so small that the practical advantages of piezoresistive readout compared to optical readout in terms of complexity and cost, as described before will compensate the smaller resolution.

3.4 Summary

In this chapter the characterization of the gauge factor and $1/f$ noise in the piezoresistors were described. In order to conclude on the best material parameters, the signal to noise ratio was calculated. It was found that highly doped and high temperature annealed single crystalline silicon exhibits the highest signal to noise ratio. Highly doped and high temperature annealed microcrystalline exhibits the highest signal to noise ratio for the polysilicon material. The dimension optimization suggested designs for optimized performance. Finally, the minimum detectable surface stress for a cantilever with optical readout was calculated and it was found that the performance is about 10 times better than for a cantilever with piezoresistive readout.

Chapter 4

Design

In this chapter the design of the chip consisting of cantilevers integrated in a microliquid handling system is presented.

The overall aim of the design is shown as a schematic in figure 4.1. The schematic shows a chip, where cantilevers are placed in a microchannel. The liquid inlet and outlet is performed from the backside. A material layer is placed on top of the substrate which defines the spacing between the cantilevers and a lid. It is seen from the

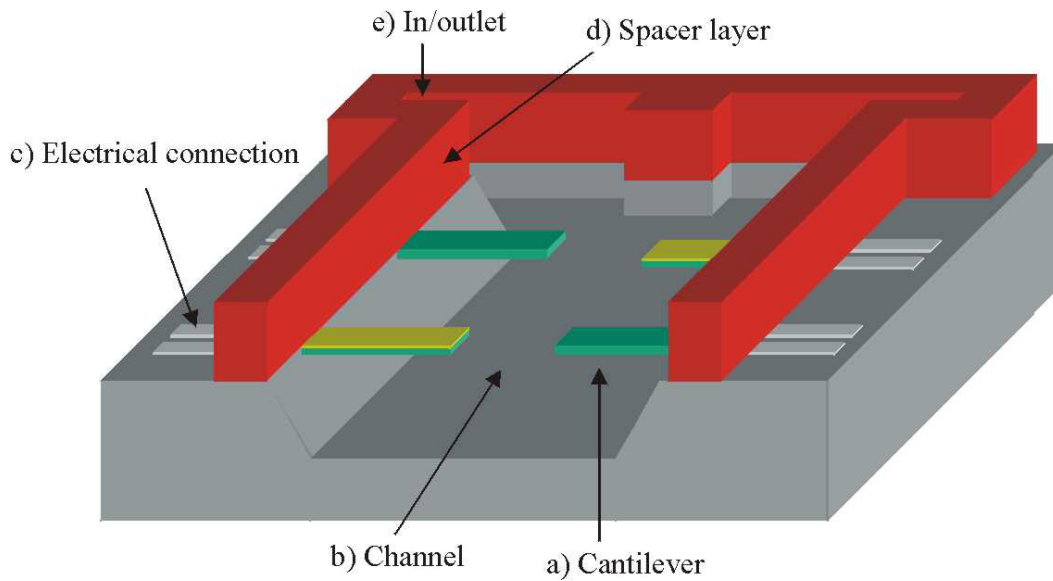


Figure 4.1: The picture shows a schematic of the chip. Basically, it is necessary to design the chip with respect to: a) the cantilevers, b) the channel, c) the electrical connections, d) the spacer layer and finally, e) the inlets and outlets.

figure that it is necessary to design the chip with respect to: a) the cantilevers, b) the channel, c) the electrical connections, d) the spacer layer and finally, e) the inlets and outlets.

The design considerations for making the chip are discussed. First, the cantilever design is presented and the expected performance with respect to change in surface stress change sensitivity is calculated. Hereafter, the channel is designed with respect to laminar flow. Different chip designs are discussed and the masks are presented. Finally, considerations due to back-end processing are discussed.

4.1 Electrical design

The electrical readout system is based on a Wheatstone bridge, where a change in resistance in a resistor is transformed into an electrical signal. The Wheatstone bridge design used in this thesis was first presented by A. boisen in [1]. The design includes an *on-chip* Wheatstone bridge with two of the resistors placed on cantilevers and two resistor placed on the substrate, see figure 4.2. One of the cantilevers is then

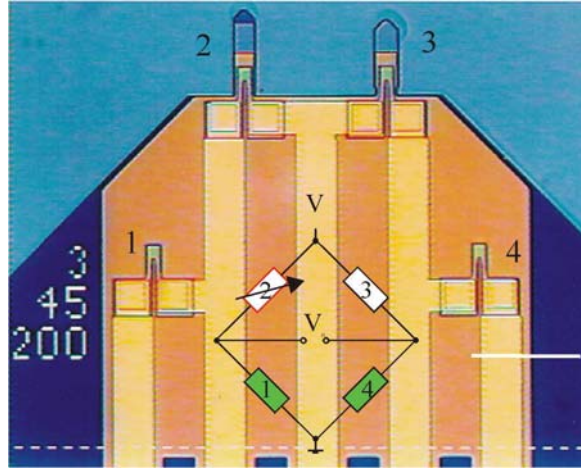


Figure 4.2: A schematic of the on-chip Wheatstone bridge, where two of resistors are placed on cantilevers and the other two on the substrate. The numbers 2 and 3 indicate the cantilever resistors whereas 1 and 4 indicates the substrate resistors.

used as a measurement cantilever, while the other is used as a reference. During measurement the two cantilevers are exposed to the same physical environment, such as temperature, mechanical noise from the surroundings, turbulence in the liquid and changes in the viscosity of the liquid. Changes in the resistance due to changes in the physical environment are then cancelled in the Wheatstone bridge. The drift reduction due to the reference cantilever has been investigated by J. Thaysen [19] and was found to reduce the drift a factor of hundred compared to a system without a reference cantilever. L. Christensen [91] has investigated the noise reduction due to the reference cantilever. Figure 4.3a shows the signal from the measurement cantilever during an alcohol detection experiment, it is seen that the signal is very noisy. In figure 4.3b the signal from the reference cantilever is shown which is also very noisy. The signal obtained from subtracting the reference signal from the measurement signal is shown in figure 4.3c which significantly increased the signal to noise ratio. Finally,

the signal obtained directly from the configuration with the *on-chip* filter is shown in figure 4.3d. It can be seen that the signal to noise again has increased about a factor of two compared to (c). In all, the *on-chip* filter has increased the signal to noise ratio by a factor of 25.

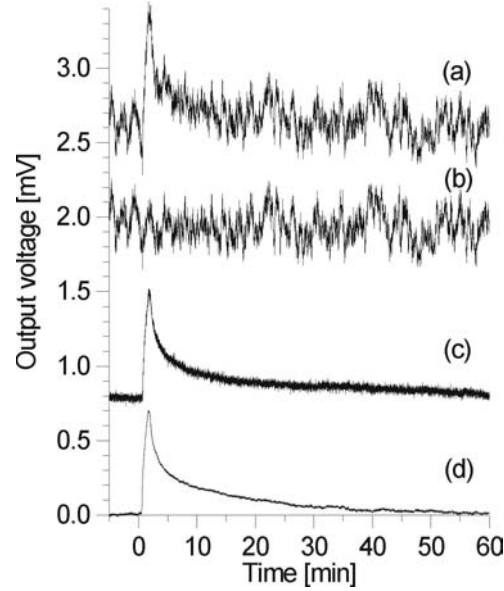


Figure 4.3: Noise reduction due to the mechanical *on-chip* filter. a) shows the signal from the measurement cantilever, b) shows the signal from the reference cantilever c) shows the signal when subtracting the signal from the reference cantilever from the measurement cantilever. Finally, d) shows the signal from the *on-chip* filter.

4.2 Cantilever design

The gauge factor and $1/f$ noise characterization were performed after the design was chosen and the fabrication of the chip started. Therefore, the finished chips do not reflect the results obtained during the parameter characterization and optimization. During the design of the cantilever a severe mistake was done, since the piezoresistor was placed on the opposite side of the neutral axis with respect to the metal layer at which the surface stress change is supposed to act. The reason for that was simply that the theory at that point was not completely developed and it was assumed that the surface stress would apply a symmetric strain in the cantilever around the neutral axis. Due to some fabrication considerations, which will be discussed later, it was decided to place the piezoresistor on the wrong side on the neutral axis. Nevertheless, as a demonstrator of the principle the chip will work perfectly.

It was decided to use polysilicon piezoresistors even though they exhibit lower signal to noise ratio than single crystalline silicon resistors. This was done since polysilicon

resistors fully encapsulated in silicon nitride are much easier to fabricate than fully encapsulated single crystalline silicon resistors, which requires the use of an SOI wafer. A cross section of the cantilever is shown in figure 4.4. The gold layer, placed on the top

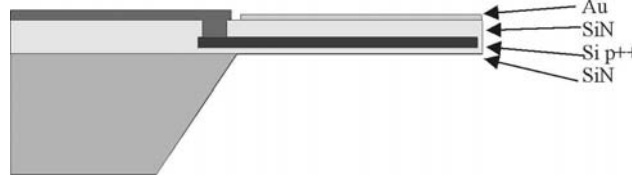


Figure 4.4: A cross sectional schematic of the cantilever with integrated piezoresistors.

of the cantilever is used for the immobilization of molecules. The material thickness and parameters are given in table 4.1. The thickness of the thin films were found by optimizing the surface stress sensitivity. The optimization with respect to noise was only performed by assuming that the noise increases as a function of the square root of the resistor thickness. As seen, the layer thicknesses are quite close to the optimized cantilever layer thickness given in table 3.7, except for the misplacement of the resistor.

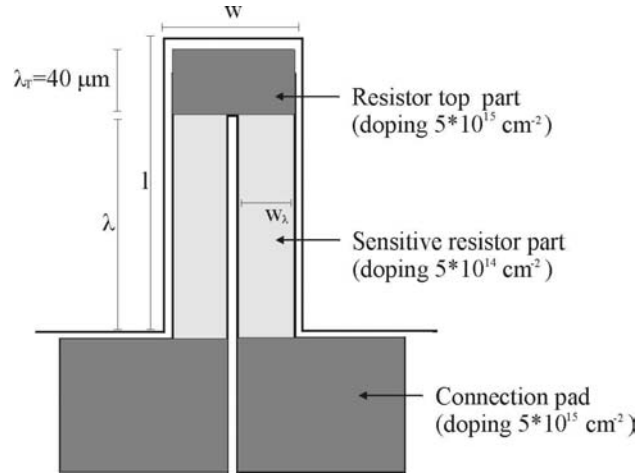


Figure 4.5: A schematic top view of the cantilever with integrated piezoresistor.

Figure 4.5, shows a top view of the cantilever with integrated resistor. The top part of the resistor is doped a factor of 10 times higher than the rest of the resistor in order to minimize the transversal contribution to the change in resistance, see equation 2.2-1. The resistor is designed with amorphous silicon doped with a dose of $N_D = 5 \cdot 10^{14} \text{ cm}^{-2}$ and annealed at 835°C in 1 hour. Three different cantilever dimensions have been designed, see table 4.2. The calculated spring constant, resonant frequency, surface stress sensitivity and the minimum detectable surface stress are presented in table 4.3. Design 4 has the same dimensions as design 1. The only difference is that the resistor is placed on the right side of the neutral axis. It is seen that the minimum detectable

Thin film	$h[nm]$	$E[GPa]$	$\sigma[MPa]$	$\rho[kg \cdot m^3]$
Au	40	79	35	19281
Si_3N_4	280	250	50	3100
$Si p^{++}$	150	180	-10	2330
Si_3N_4	50	250	50	3100

Table 4.1: Design parameters. The thickness of the thin films was found by optimizing the surface stress sensitivity, (with the surface stress placed on the opposite side of the neutral axis.)

Design	$l[\mu m]$	$w[\mu m]$	$\lambda[\mu m]$	$w_\lambda[\mu m]$
1	120	40	100	2x17
2	80	40	60	2x17
3	120	60	100	2x27

Table 4.2: Three different cantilever designs is included in the chip design.

surface stress in design 1 is approximately a factor of 4 larger design 4. Design 4 has not been fabricated and the parameters are only listed as comparison to the other designs.

4.3 Chip design

Five different chip designs have been realized. The overall design, such as the chip size and the channel dimensions have not been changed, but only the placement of cantilevers, the cantilever dimensions, see table 4.2, and the number of reference cantilevers. As an example of the chip design, chip A is shown in figure 4.6, with applied chip dimensions. It is seen that the chip size is designed to $A = 6.1 \times 6.1 \text{ mm}^2$, the reason for this size will be given in the following section, concerning the back-end processing. In the chip design A, 10 cantilevers are placed in the channel, with a spacing of $s = 400 \mu m$. Half of the cantilevers are used for measurements, while the other half are used as references. The measurement cantilevers are defined as the gold coated cantilevers. Some of the other designs, do not have the same spacing and the same

Design	$\frac{\Delta R}{R}/\sigma_s [m/N]$	$\sigma_{s,min} [N/m]$	$k [N/m]$	$f_{res} [kHz]$	$\frac{\Delta R}{R}/z [nm^{-1}]$
1	$1.9 \cdot 10^{-4}$	$1.2 \cdot 10^{-2}$	0.16	41	$-0.5 \cdot 10^{-6}$
2	$1.9 \cdot 10^{-4}$	$1.6 \cdot 10^{-2}$	0.54	92	$-1.0 \cdot 10^{-5}$
3	$1.9 \cdot 10^{-4}$	$9.7 \cdot 10^{-3}$	0.24	41	$-0.5 \cdot 10^{-6}$
4	$7.2 \cdot 10^{-4}$	$3.2 \cdot 10^{-3}$	0.16	41	$0.5 \cdot 10^{-6}$

Table 4.3: Theoretical performance of the cantilever designs. Design 4 has the same dimensions and cantilever material thicknesses as design 1. The only difference is, that the resistor is placed on the right side of the neutral axis. The gauge factor and α factor used are obtained from the low doped low annealed amorphous silicon in table 3.1 and 3.4.

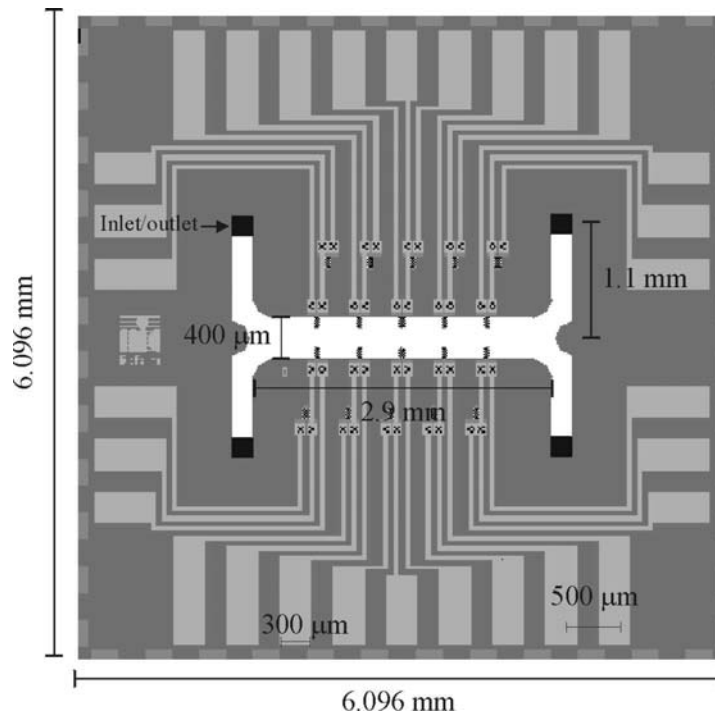


Figure 4.6: A schematic top view of chip A with the chip dimensions.

Chip design	Cantilever design	$s[\mu m]$	Reference cantilever
A	1	400	2,4,6,8,10
B	2	400	2,4,6,8,10
C	3	400	2,4,6,8,10
D	1	400	3,10
E	1	212	2,4,6,8,10

Table 4.4: The five different chip designs. s indicates the spacing between the cantilevers.

number of reference cantilevers, in order to investigate the performance with respect to these parameters, see table 4.4.

4.4 Channel design

A major goal in this thesis is to integrate cantilevers into a microliquid handling system. The reasons for integrating the cantilevers into a very small channel are many. First of all, the small volume of the interaction chamber will significantly decrease the amount of test sample needed. The flow in micrometer sized channels can for reasonably flow rates be considered laminar. This will decrease the noise in the system since noise from turbulence is eliminated. Finally, temperature gradients in the interaction chamber, causing long stabilization time before starting a measurement are also minimized. In this section the design of the micro channel is presented, which fulfills the requirements

of low volume and liquid flow in the laminar regime, even with cantilevers placed in the channel. In the following subsection a very short overview of the flow theory is presented. This will show that the flow is always laminar in a microchannel.

4.4.1 Laminar flow in a channel

A theory concerning viscous fluid flow was developed by Navier in 1827 and Stoke in 1845. They expressed their rather complicated theory in the fundamental Navier-Stoke equation. The Navier-Stoke equation is the fluidic version of conservation of momentum, and is derived from Newton's second law, $F = ma$. In order to investigate the flow in a channel, some assumption has to be made in order to simplify the Navier-Stoke equation. Therefore, only incompressible fluids, i.e fluid with constant density is considered. It is further assumed that the viscosity η of the fluid is independent of pressure and temperature. Frank M. White [92] has in his book "*Viscous Fluid Flow*" suggested a useful way to express the Navier-Stoke equation in terms of dimensionless variables, and neglecting the gravitational effects

$$\rho^* \frac{dV^*}{dt^*} = -\nabla^* P^* + \frac{\eta_0}{\rho_0 V_0 L_{ref}} \eta^* \nabla^{*2} V^* \quad (4.4-1)$$

where the dimensionless variables are indicated with *. η_0 is the free-stream viscosity, ρ_0 is the free-stream density, L_{ref} is a characteristic length, V_0 is the reference velocity, V is the velocity and P the pressure drop over the considered system. The left side of the equation can be viewed as the inertial forces, while the last part of the right side can be viewed as the viscous force. By introducing the Reynolds number Re given as

$$Re = \frac{\rho_0 V_0 L_{ref}}{\eta_0} \quad (4.4-2)$$

it is seen that if $Re \ll 1$ the viscous force term will dominate the dynamics of the fluid and will be balanced by the pressure force. The inertial forces, $\rho^* \frac{dV^*}{dt^*}$, which causes the turbulence can be neglected and the flow can be considered laminar. Experience shows that laminar flow is obtained for Reynolds numbers up to $Re \approx 2300$.

Assume that the channel is rectangular with the cross-sectional area $A = H \cdot W$, where H is the channel height and W is the channel width. An estimate of the characteristic length can be found from the hydraulic parameter D_h given by [92]

$$L_{ref} = D_h = \frac{4A}{Wetted\ perimeter} = \frac{4HW}{2(H + W)} \quad (4.4-3)$$

The wetted perimeter is the inner circumference of the channel. The hydraulic parameter can also be used to estimate the entrance length L_e , which is the length it takes before the flow is fully developed after entering the channel, see figure 4.7. Regardless of the shape of the cross section in the flow channel for laminar flow the entrance length L_e can be estimated by [92]

$$\frac{L_e}{D_h} = \frac{0.6}{1 + 0.035Re} + 0.056Re \quad (4.4-4)$$

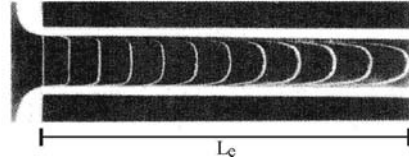


Figure 4.7: When the flow is developed the flow profile will remain constant through the channel. There is a short entrance length L_e before the flow profile is fully developed [92].

This equation states that the flow is developed a very short distance after entering the channel when the Reynolds number is low.

The Reynolds number of water flowing in a channel with the flow rate of $\Phi = 100 \mu L/min$ and the channel height of $H = 200 \mu m$ and a width of $W = 400 \mu m$, where the reference flow can be written as $V_0 = \frac{\Phi}{A}$ can be calculated to

$$Re = \frac{\rho_0 V_0 L_{ref}}{\eta_0} = \frac{\rho_0 \left(\frac{\Phi}{HW} \right) \left(\frac{4HW}{2(H+W)} \right)}{\eta_0} = \frac{2\rho_0 \Phi}{\eta_0 (H + W)} \simeq 12 \quad (4.4-5)$$

From this example it can be seen that laminar flow is obtained in such a channel even for very high flow rates. The entrance length L_e can be estimated from expression 4.4-4 to $L_e \simeq 180 \mu m$. This length is the minimum length between the flow inlet and the first cantilever in order to obtain the same flow on each cantilever.

Figure 4.8 shows a cross-sectional schematic of the channel with the cantilevers. The lower part of the channel is defined by KOH etching leaving slanted sidewalls, and can therefore not be assumed perfectly rectangular as above. Nevertheless, the calculation of the Reynolds number in equation 4.4-5 is still very close to this case, see F. White [92]. As seen in figure 4.8 the channel width and channel height is designed

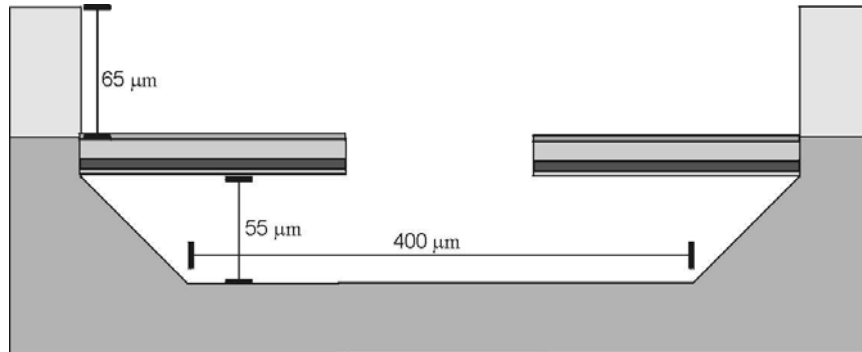


Figure 4.8: Cross sectional schematic of the channel

to $W = 400 \mu m$ and $H = 120 \mu m$. The entrance length is therefore calculated to

$L_e = 200 \mu m$ by using equation 4.4-4. As seen in figure 4.6 the entrance length is designed to $L_e = 400 \mu m$, which ensures a 100 % developed laminar flow. The channel has a length of $L = 3200 \mu m$, and a volume of $V = 0.15 \mu L$

An effect that is observed in a microchannel where the flow is laminar, is the very slow mixing of liquids. Normally, mixing is obtained via turbulence and diffusion. Since turbulence is eliminated in the laminar flow regime, mixing is only observed via diffusion which is significantly more slow than mixing due to turbulence [93]. A test has also shown that mixing in a micro channel with the above dimensions is not observed for flow rates $\Phi > 1 \mu L/min$. It is possible to flow two different liquids side by side in the channel without any mixing. This can for example be used for measuring on two different samples at the same time, or making differential measurements on two samples simultaneously. The chips are therefore designed with two inlets and two outlets, enabling two liquids in the channel at the same time. These can also be seen in figure 4.6

4.5 Back-end design

During the design of the chip, the back-end processing was taken into consideration in order to ease the use of the chip. The back-end processing includes the placement of the chip in a chip house and wire bonding from the chip to electrical contacts on the chip house. A lid has to be placed on top of the channel in order to completely seal the channel. Finally, the liquid inlet and outlet on the chip have to be connected to tubes. A commercially available chip house is used, see figure 4.9. The inner side-length of

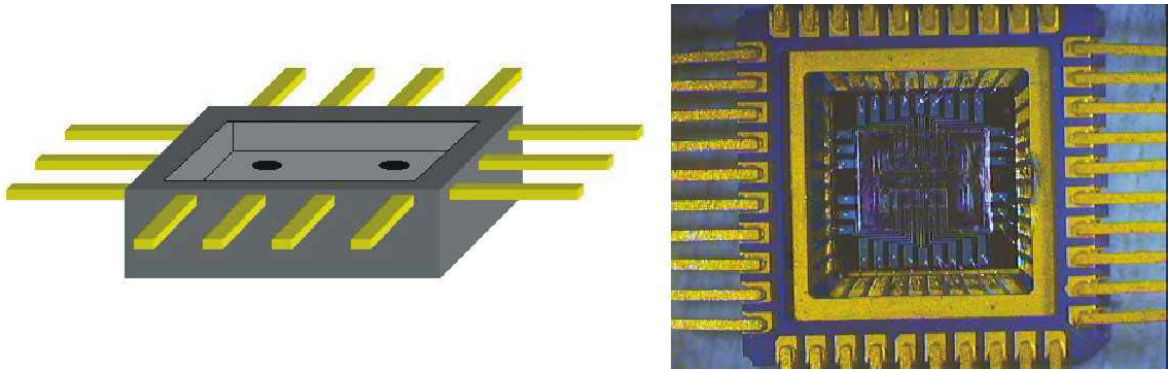


Figure 4.9: Schematic of the chip house on the left and optical image of the actual chiphouse on the right. The chip house has 40 electrical connections. The inner side length is 6.1 mm. The holes in the bottom of the chiphouse are used for the liquid in/outlets.

the chip house is 6.2 mm and the chip fits therefore perfectly into the house. 4 holes are drilled in the bottom of the chip house for the liquid connections. The chip house has 40 electrical connections, which are sufficient for the 30 electrical wires on the chip.

The placement of the electrical connection pads on the chip are designed to fit the pads on the chiphouse.

4.6 The mask design

In this section the masks are briefly described. The design includes nine masks. At this point in the thesis, there has been no argumentation for choosing a fabrication sequence that utilize the masks presented in this section. The next chapter will describe some fabrication steps that have been tested in order to choose a good fabrication sequence. The chip fabrication sequence is presented in figure 6.1 in chapter 6.

The first mask "Resistor" in figure 4.10a defines the piezoresistors. The resistors is on the cantilevers and the substrate are defined here.

In order to minimize the contribution of the transversal strain, and the resistance in the connection pads, these areas are highly doped, see figure 4.5. Mask 2 in figure 4.10b defines the implantation mask.

The third mask in figure 4.10c, is used on the back side of the wafer to define the liquid inlet and outlet. Since these are etched in KOH, the masks are larger than the actual inlet and outlets due to the etch anisotropy.

The channel, cantilever and contact holes are defined by mask 4, figure 4.10d. The 400 μm wide channel is designed such that the two in/outlet channels are exactly half the width of the channel. The flow resistance at the channel junction is therefore minimized. The distance between the first cantilever and the inlet channel is a about 400 μm . For a channel depth of 120 μm a fully developed laminar flow is obtained before reaching the first cantilever, see section 4.4.1.

Mask 5 in figure 4.10 defines the protection of the contact holes, and the larger patterns are used for corner compensations during the anisotropic KOH etching. These corner compensations are designed such that the KOH etched side wall follows the corners of the channel junction defined in mask 4.

Mask 6 defines the immobilization metal on the measurement cantilever, while mask 7 defines the metal on the reference cantilevers. As seen in the mask, every second cantilever is used as measurement cantilever.

The electrical connections to the piezoresistors are defined in mask 8, figure 4.10h. The mask is made symmetrical around the center.

Mask 9 in figure 4.10i is used for the upper part of the channel fabricated in the polymer: SU-8.

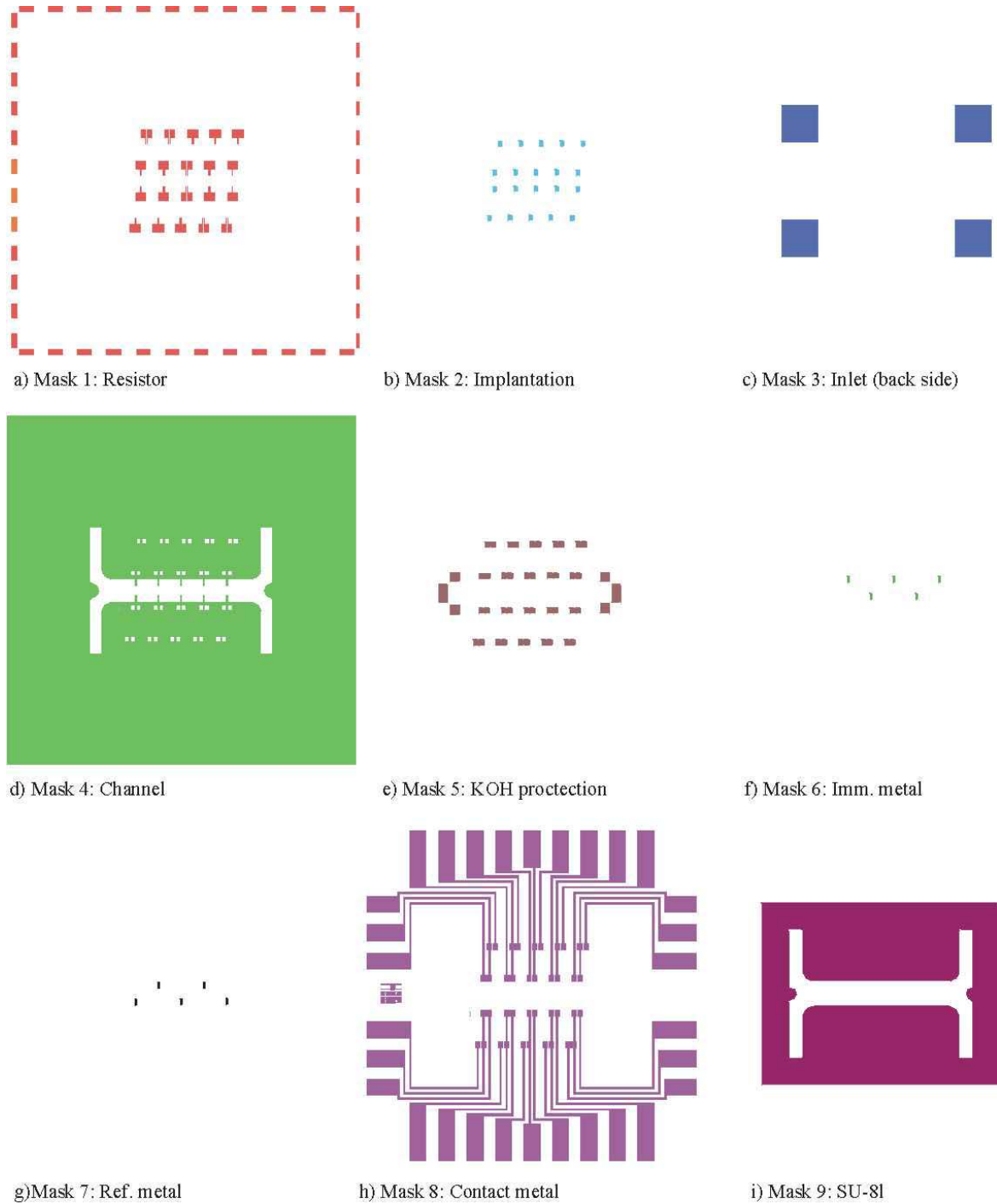


Figure 4.10: The mask layout for making the cantilevers with piezoresistive readout integrated in a microliquid handling system. Nine masks are used for the fabrication of the chip.

4.7 Summary

In this chapter the design considerations have been discussed. First, the Wheatstone bridge with build-in filter was presented. The cantilever designs were presented and

the performance calculated. Unfortunately, the piezoresistor was placed on the wrong side of the neutral axis with respect to the surface stress, which yielded a theoretical performance 4 times less than originally expected. A short introduction to fluid mechanics was presented. From this, it could be concluded that the flow is in the laminar regime for reasonable flow rates. A chip consisting of 10 cantilevers with piezoresistive readout inserted in a channel is designed with four in/outlets. The back-end processing was discussed and the masks for the fabrication were presented.

Chapter 5

Fabrication technology

In this chapter, tests of some of the fabrication process steps are described. These tests have been performed prior to the design and process sequence for the chip. The tests were made in order to choose the best solutions for designing and fabricating the chip, with respect to high yield and a low number of critical fabrication steps. The reasons for most of the tests might at this point in the thesis be a little unclear, but these investigations are justified during the chip fabrication described in the following chapter.

In figure 5.1 a schematic of the chip is presented. Basically, the chip consists of 5 different building blocks: a) the cantilevers, b) the channel, c) the electrical connections, d) the spacer layer and finally, e) the inlet and outlets. The fabrication technique for each

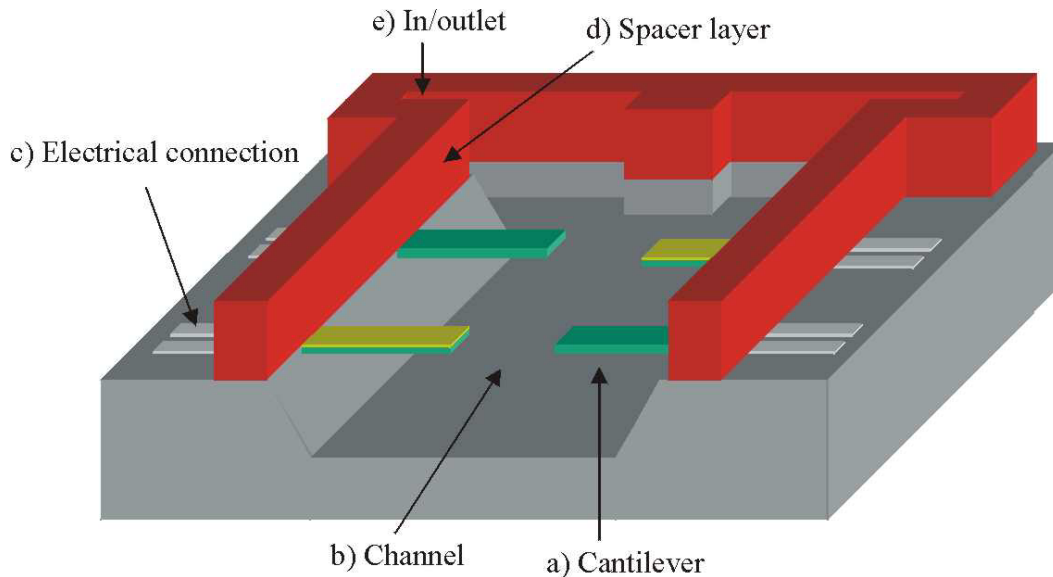


Figure 5.1: The picture shows a schematic of the chip. Basically, the chip consists of 5 different building blocks. a) the cantilevers, b) the channel, c) the electrical connections, d) the spacer layer and finally, e) the inlet and outlets.

of these building blocks separately, is more or less well-known. The challenge occurs when all the building blocks have to be merged in order to fabricate a well-functioning chip.

The first test described is investigating the different channel definition possibilities. Hereafter, the problem of metal deposition on free hanging cantilevers and deposition of metal for electrical contacts are described. Finally, the polymer SU-8 is tested for its suitability in the fabrication process.

5.1 Etching of the channel

The etching of the channel is one of the more complicated steps to be considered in this thesis. The basic etching is not complicated, but in fact there are only two methods available, dry etching, using for example RIE, or wet etching using for example KOH. Since the cantilevers also need to be released without any significant damaging during the channel etching, the etching gets more complicated. The immediate conclusion is that the channel etching should be done in the very last fabrication step since it is difficult to perform further processing on free hanging cantilevers. Another issue that needs to be addressed is that the cantilevers need to be placed in the middle of the channel side wall. Therefore a material has to be placed on top of the substrate in order to define the upper part of the side wall.

The obvious solution for the definition of the upper part of the channel wall and also the definition of the channel lid is to bond a glass wafer on top of the cantilever chip wafer after the channel etching. It was decided not to use this method for several reasons. The main reason is, that it is necessary to be able to address each individual cantilever on the finished chip. This might be necessary during immobilization of molecules onto the cantilevers, depending on the immobilization method. One method is the "ink jet" technique [94], where each cantilever is spray coated with a specific type of molecule. The molecules could for example also be deposited before the bonding is performed, but since anodic bonding normally is performed at 300-400 °C [95], the bio-molecules will probably not survive the bonding. Thus, it is decided to design the chip without any lid. Another reason for not choosing the anodic bonding technique is that very flat surfaces are needed in order to perform this bonding. This requires that the electrical connection wires are at the same level as the substrate, or that buried resistors are used, which will make the fabrication process more complicated.

Electroplating of nickel is also a candidate for the definition of the upper part of the side wall. This technique has for example been used to fabricate all-metal AFM probes [96]. Since electroplating of nickel requires the electrical connections to the resistors to be isolated, it was decided not to use this method either. Another disadvantage is, that nickel might react with thiol-groups, used for the molecule immobilization on gold coated cantilevers. Since the side wall area is much larger than the cantilever area most of the molecules would react with the side wall instead of with the cantilever

surface, which would impede the experiments.

The photo-resist called SU-8, has during the last couple of years shown to be a very strong tool for high aspect ratio microfabrication structuring [97, 98]. SU-8 is a negative, epoxy-type, near-UV photoresist. The SU-8 resist allows a broad range of thicknesses to be obtained with only one spin process. Thicknesses between 750 nm and 200 μm have been obtained [99]. After cross-linking, SU-8 is very difficult to remove due to its excellent chemical resistance.

The fact that SU-8 is simply spun on the wafer, structured by conventional photolithography technique, whereafter it is developed leaving structures nearly impossible to remove makes the SU-8 a very strong candidate for the definition of the upper part of the channel wall. Thus, it was decided to use SU-8 as the upper part of the side wall.

5.2 Channel etching by RIE

In this section the channel definition by use of reactive ion etching is described. As described in chapter 4 the cantilever material is silicon nitride. In order to release the cantilevers during the channel etching by RIE an isotropic silicon etch is required. The RIE system at MIC offers an isotropic etch by a SF_6 -gas, described by B. Andersen in [100]. The isotropic etch has a selectivity of approximately 50 over silicon oxide, a selectivity of approximately 7 over resist, and 10 over silicon nitride.

It is therefore necessary to protect the silicon nitride on the cantilever and on the substrate during the isotropic reactive ion etching of the silicon. Since the SF_6 does not attack aluminum, aluminum can be used as mask material. In figure 5.2, the process sequence for the RIE test is shown. Since the isotropic etch also attacks the silicon nitride from the backside, a 2 μm thick silicon oxide is first deposited on a wafer, see figure 5.2a. In order to simplify the test, the silicon oxide is also used as the cantilever material. A test mask defining the cantilever and the substrate is transferred to the wafer by conventional photolithography technique. The cantilever is then etched in BHF. After stripping the resist (5.2b), the protective aluminum layer is deposited on the cantilever and substrate using lift-off technique (5.2c). The channel is then etched and the cantilevers are released in the isotropic silicon etch (5.2d), leaving a 50 μm deep channel.

Figure 5.3 shows SEM micrographs of the finished channel and free hanging cantilevers after isotropic etching and subsequent removal of the aluminum. Since the cantilever thickness can be measured to about 2 μm it can be concluded that the isotropic etch attacks the silicon oxide very slowly from the backside of the cantilever. It is also observed that the cantilevers exhibit a shadowing effect leaving 10 μm high structures below the cantilevers. These shadow structures might turn out to be a problem when flowing a liquid through the channel, since the structures can be seen as flow resistances and together with the cantilevers these might act as "bubble collectors". As expected,

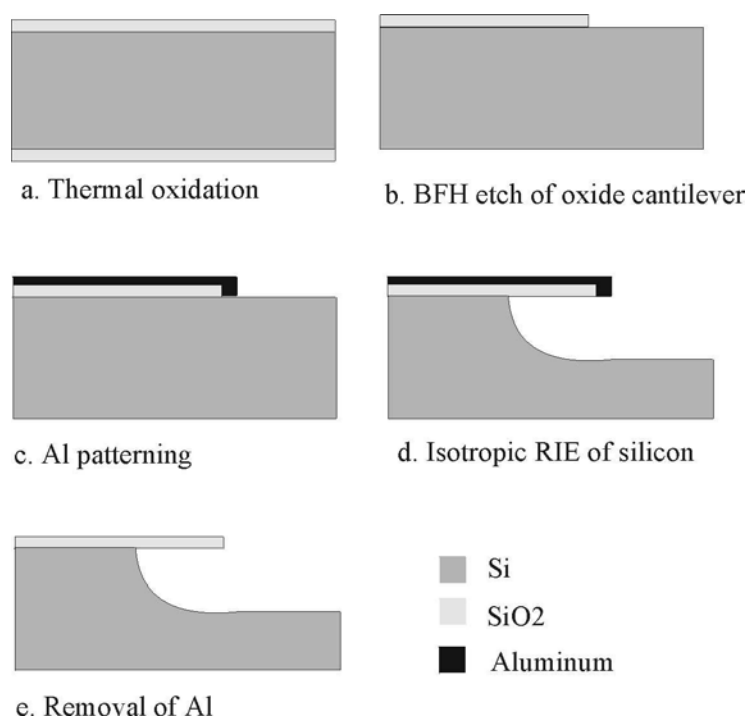


Figure 5.2: The process sequence for testing the reactive ion etch procedure of the channel and releasing the cantilevers.

it is also seen from the micrograph that the reactive ion etching will under-etch the substrate resulting in a poor non-defined cantilever clamping. This might not be a problem however, since the cantilever clamping could be performed by the SU-8 side wall on the upper side.

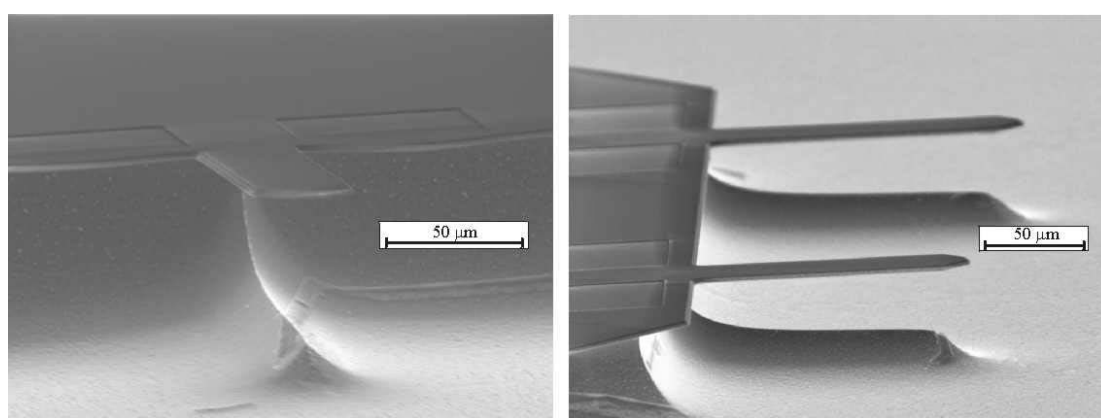


Figure 5.3: SEM micrographs of the reactive ion etched channel. A shadowing effect is observed, which results in 10 μm structures below the cantilevers.

Another concern regarding RIE of the channel is related to the masking material. In the test aluminum exhibited a very good masking behavior, but the e-beam deposition profile of the aluminum, has a very poor step coverage, see figure 5.4. When depositing the aluminum on the cantilever the edge of the cantilever is not covered perfectly, and the silicon nitride on the edge of the cantilever might therefore be etched, leaving a non-protected resistor. This could not be concluded from the test, since the isotropic

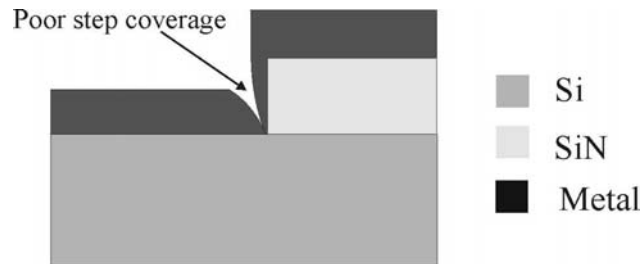


Figure 5.4: *Cross-sectional view of the step coverage when depositing metal using e-beam evaporation technique. It is seen that the step coverage is very poor.*

etch etches the silicon oxide very slowly. The black color defining the transition from the cantilever to the aluminum over-hang in figure 5.5 indicates that the aluminum mask is under etched at the cantilever edge. Photoresist is another possible mask

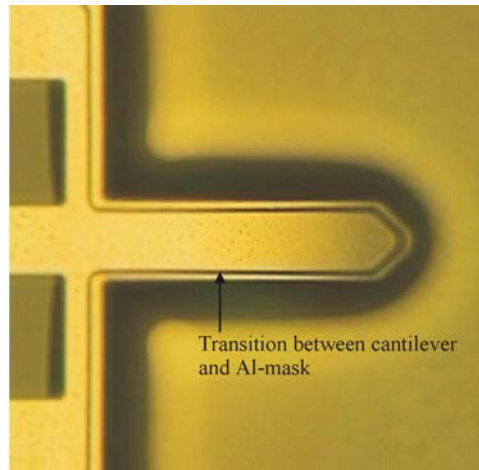


Figure 5.5: *The photograph shows the cantilever before the removal of the aluminum mask. The thick black line indicating the transition between the cantilever and the aluminum mask indicates an under etch.*

material. Photoresist was not considered in the test. When using photoresist as an etch mask the 50 μm thick SU-8 needs to be deposited before the photoresist. Thus, it is believed that it will be difficult to completely cover the areas close to the SU-8.

5.2.1 SU-8 compatibility with RIE

The literature does not report on etch rates of SU-8 in SF_6 based reactive ion etching. The etch-rates in silicon and SU-8 are therefore investigated. The etch-rate test also determines how the SU-8 will react to RIE. The elevated temperature during the etching might increase the build-in stress in the SU-8 which could leave to poor adhesion between the substrate and the SU-8.

50 μm thick SU-8 is first spun, and patterned on a wafer with a 2 μm thick silicon oxide. The silicon oxide is then etched in BHF, whereafter the channel is etched in RIE. The recipe is 40 sccm SF_6 at a pressure of 80 mbar. The wafer is etched for 2 hours. The result is seen in figure 5.6. After the etch the adhesion between the substrate and SU-8 was good. The etch rate of the silicon was measured to $er_{Si,v} = 0.5 \mu m/min$ and $er_{Si,h} = 0.25 \mu m/min$ for the vertical and horizontal direction, respectively. The isotropic etch rate of the SU-8 was measured to $er_{SU-8} = 50 nm/min$, yielding a selectivity of 1:10 between SU-8 and silicon.

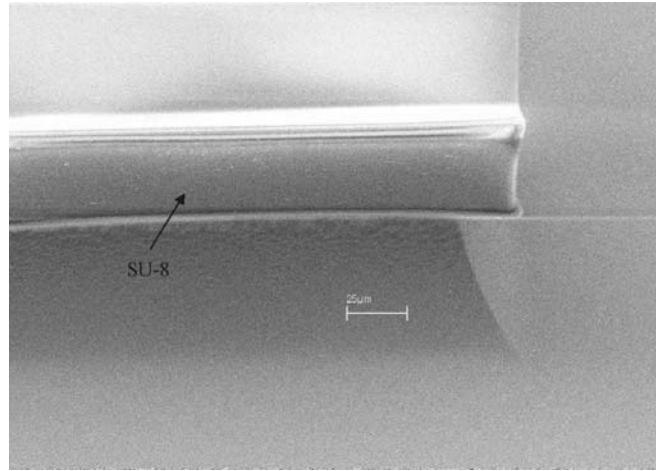


Figure 5.6: SEM micrograph of reactive ion etched channel with SU-8 as a mask layer. The selectivity in etch rates between SU-8 and silicon is found to 1:10

5.3 Channel etching by KOH

Anisotropic etching of silicon using KOH is often used when fabricating micromechanical structures in silicon. The anisotropy is dependent on the crystal planes, thus the ratio of the etch rates for the (100)-, (110)-, and (111)-planes is in index number 100:16:1. When KOH etching $\langle 100 \rangle$ -oriented silicon through a silicon nitride mask, precise V-shaped grooves are etched, with the (111)-planes defining the edges at an angle of 54.7° .

The etch rate of the (100)-plane in silicon is about $0.8 \mu\text{m}/\text{min}$ at $T=70^\circ\text{C}$ in 28 % KOH, whereas the etch rate of silicon nitride is less than $0.3 \text{ nm}/\text{min}$. Therefore KOH etching is a very good candidate for etching the channel, since the cantilevers can be released without any masking of the silicon nitride. A test of releasing the silicon nitride cantilevers by KOH etching also showed that free hanging cantilevers can be obtained without any shadow structures below the cantilevers.

The disadvantage of using a KOH etched channel is, that the SU-8 structures do not adhere to the substrate after the KOH etching. The SU-8 itself is not etched, but it is lifted from the substrate. Therefore the SU-8 has to be deposited and structured after the KOH etching. This means that the SU-8 has to be spun on a very structured surface with free-hanging cantilevers. To the authors knowledge such a technique has not previously been described in the literature. Some other problems that also need to be addressed concerns the protection of the silicon in the contact holes and the metal on the cantilevers during the KOH etching.

5.3.1 Electrical connections

In order to obtain electrical contact to the silicon resistors, contact holes are opened in the silicon nitride. The electrical connections are then defined by deposition and structuring a metal layer. The process sequence for this procedure can be seen in figure 5.7. After fully encapsulating the resistor in silicon nitride (figure 5.7a), a contact hole is made in the silicon nitride by RIE (5.7b). A resist mask is structured for the electrical connections. A metal layer is evaporated onto the wafer and the electrical connection is defined by lift-off technique (5.7c). Due to a poor step coverage of the

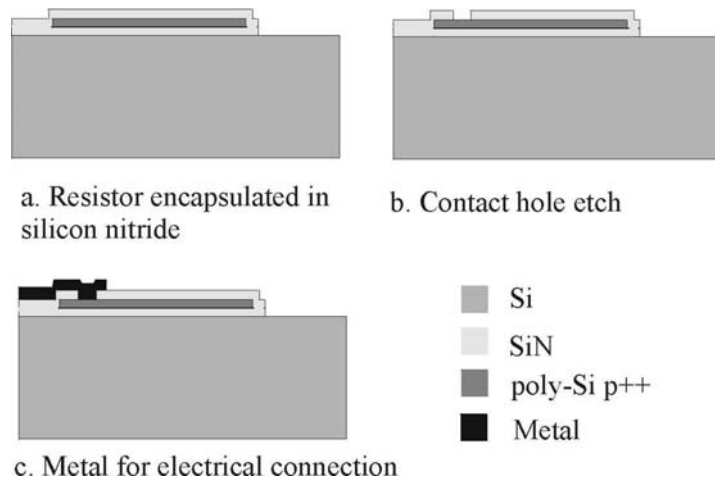


Figure 5.7: The process sequence for making electrical contacts to the silicon resistors through a contact hole

metal e-beam evaporation depositing technique, see figure 5.4, the silicon in the contact holes is etched when exposed to 70°C 28 % KOH for more than 30 min. The

metal used for the electrical connection in the test is chromium/gold, with a thickness of 2 nm / 300 nm. These layers are known to withstand KOH etching [101]. Figure 5.8 shows how the KOH has etched the silicon in the contact holes due to a poor step coverage of the metal. The yield of well protected contact holes after KOH etching for 70 min at 70 °C was about 50 %. Tests with even thicker metal layers did not show

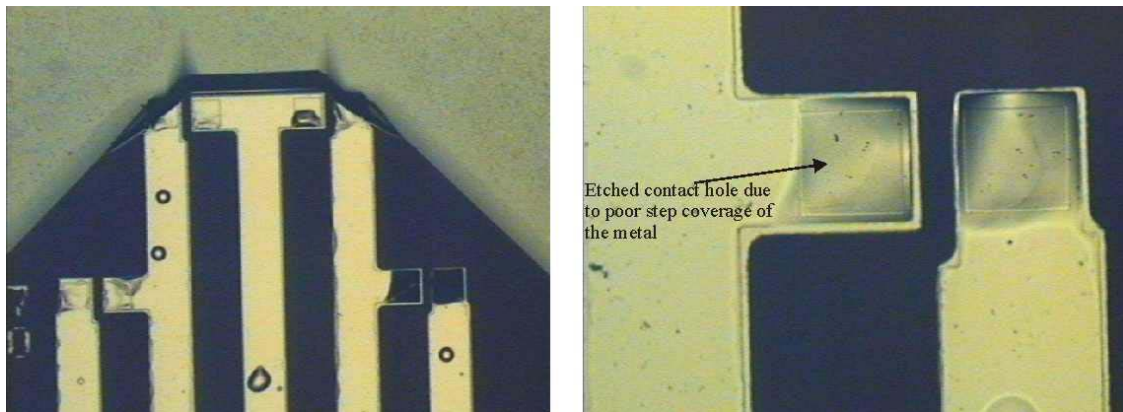


Figure 5.8: From the optical photograph it is seen that the silicon in the contact holes is etched during the 70 min long KOH etching at 70 °C

any significant increase in the survival rate of the silicon in the contact holes.

The test shows that the contact holes can first be defined and etched after the KOH etching, thus spinning resist and making photolithography on free hanging cantilevers will be necessary. A test is therefore performed in order to investigate whether it is possible to spin resist on free hanging cantilevers without breaking them.

Free hanging cantilevers, defined in 500 nm thick silicon nitride and released by KOH etching for 70 min at 70 °C were fabricated. The AZ5214 resist was spun on the wafers, yielding a thickness of 4.2 μm and a mask defining the metal connections was transferred to the wafer by photolithography. In normal conditions, i.e. a flat surface, the required exposure dose is 150 mJ/cm^2 for a 4.2 μm thick resist. But since the surface is structured with a 50 μm deep channel and free hanging cantilevers, a much thicker resist layer is trapped in the channel and especially under the cantilevers. Figure 5.9 shows a cross-sectional schematic of the channel. The resist profile is very dependent on the position in the channel. Far away from the channel the resist thickness is 4.2 μm , close to the channel the thickness is less than 4.2 μm and in the channel the thickness is much larger than 4.2 μm , even up to 25 μm . Therefore a much higher exposure dose is required in order to remove all of the resist in the channel.

The test showed surprisingly that it is possible to spin resist, align a mask and expose and develop the resist on top of a wafer with free hanging cantilevers in a 50 μm deep channel with a yield of 100 %.

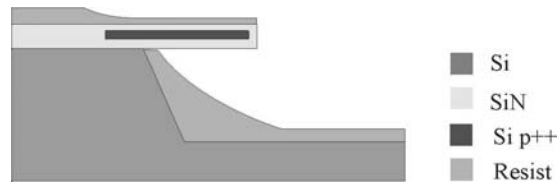


Figure 5.9: Cross-sectional schematic of the resist profile. The resist thickness is much larger than $4.2 \mu\text{m}$ in the channel.

The first idea was to use a lift-off technique in order to define the metal wires, but this turned out to simply brake off the cantilevers when exposed to ultra-sonic aggitated acetone. The solution - except for shadow masking, which has not been considered - is to deposit metal all over the wafer, including the etched channels and thereafter deposit and pattern a resist layer mask. The resist is then used as a mask in a metal etch. In order not to leave any metal in the channel after defining the metal wires it is necessary to remove all the resist in the channel. An optimization was performed in order to find the right exposure energy. The energy should be just enough to remove the metal in the channel with out loosing too much line width.

Figure 5.10 shows the results after exposing the resist with different amounts of energy and developing for 3 minutes. The left picture shows the result when using an exposure dose of $150 \text{ mJ}/\text{cm}^2$. It can be seen that there is a shadow around the cantilevers, which is non-removed resist. The right figure shows the result after an exposure energy of $1250 \text{ mJ}/\text{cm}^2$. It is seen that all the resist around and under the cantilevers has been removed in the developer. The decrease in linewidth with respect to the mask is about $15 \mu\text{m}$. From this result, it can be concluded that the exposure energy has to be increased by a factor of 8 compared to the standard recipe in order to remove the resist in the channel.

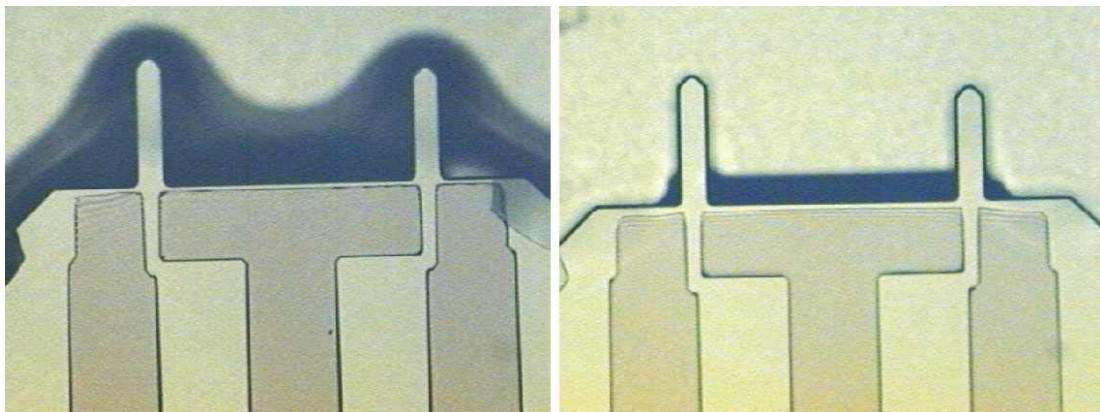


Figure 5.10: The left figure shows the result, when using a too small exposing energy while the correct amount of energy is used in the right picture

The used process sequence for defining the electrical contacts to the resistors can now be presented. The schematic of the process sequence is given in figure 5.11. The channel and cantilevers with integrated resistor are pre-defined (5.11a). The contact holes are then defined using RIE (5.11b). Next, a tetraethylorthosilicate (TEOS) silicon oxide is deposited on the wafer, and patterned by BHF-etching such that the TEOS oxide is only present in the contact holes (5.11c). The channel etching and the release of the cantilevers are performed in KOH whereafter the TEOS oxide is removed in the contact holes using BHF (5.11d). The electrical connection are defined by first depositing metal on the wafer, whereafter the electrical connection are defined as described above (5.11e). The resist mask for the metal etch is removed in acetone without ultra sonic agitations.

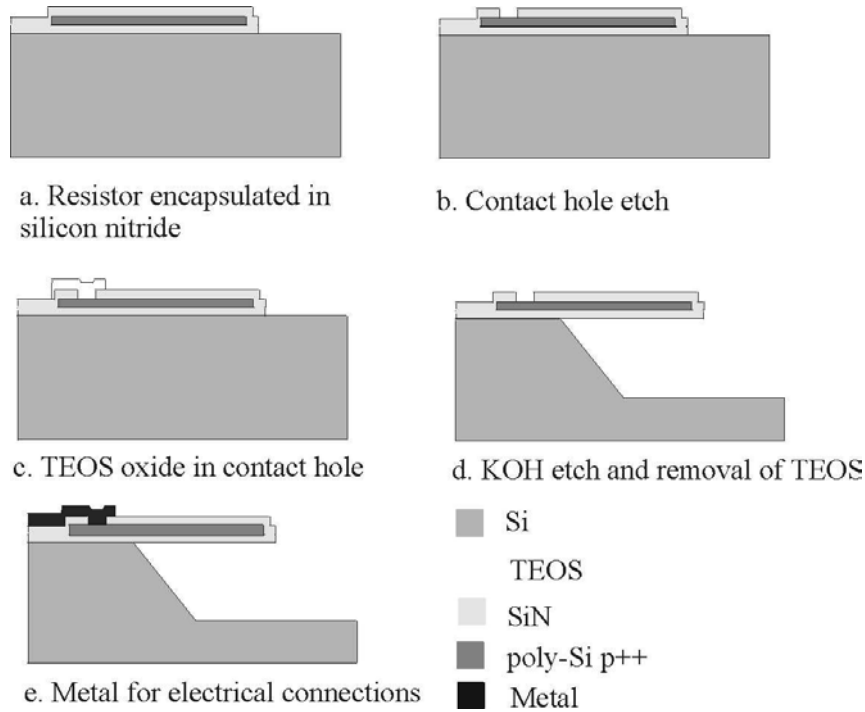


Figure 5.11: Process sequence for defining metal connections to the piezoresistors on already free hanging cantilever.

5.3.2 Metal on free hanging cantilevers

Molecules with a thiol-group are known to bind very strongly to gold. In this thesis, it has been decided to use this principle for the immobilization of bio-molecules to the cantilever. The technique is very generic, since it is possible to bind a thiol-group to almost any other bio-molecule, e.g. a DNA molecule. It is therefore necessary to deposit gold on the measurement cantilever. The gold coated measurement cantilever reacts slightly different to changes in the surroundings compared to the non-coated

reference cantilever, due to their different compositions. The gold coated cantilever is for example more sensitive than the reference cantilever to changes in the temperature due to the bimorph effect. The quality of the build-in filter is therefore reduced.

The reference cantilever can in principle be coated with another metal, which exhibits the same characteristics as gold with respect to thermal expansion coefficient and Young's modulus. Of course the metal should be chosen such that the bio-molecules exhibits a very weak binding to this metal. If the metal is deposited on the cantilever before the KOH etching of the channel, the number of available candidates for the reference metal is severely reduced, since many metals are etched in KOH. The only metals available at MIC which withstand KOH etching are gold, chromium, nickel and platinum. None of these material fulfills the above described characteristics.

In order to increase the number of candidates to the reference metal, a test was performed in order to investigate if it is possible to coat and mask free hanging cantilevers. As described in section 5.3.1, it is not possible to define metal structures by use of lift-off technique, since the ultra-sonic assisted acetone bath breaks the cantilevers. Lift-off with-out using ultra-sonic agitated acetone did not give a good result. Metal is therefore deposited all over the wafer whereafter the metal is etched away except at places protected by a resist mask. In figure 5.12 an optical image shows a resist mask on a cantilever. The resist mask is severely degraded due to the heavily over-exposure in order to remove the resist in the channels. The result shown in the figure was the best obtained by this method, and it was concluded that it is not possible to define patterns on free hanging cantilevers.

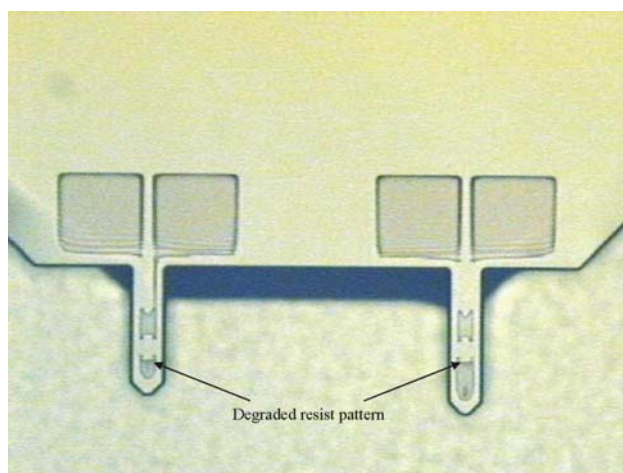


Figure 5.12: Optical image of resist patterns on free hanging cantilevers. The pattern is heavily degraded, and defining structures on free hanging cantilevers is therefore not possible, using conventional photoresist patterning technique.

It is very difficult to find a metal that exhibits the same characteristics as gold with

respect to thermal expansion coefficient and Young's modulus. At the same time it is required that the metal is inert to thiol-group immobilization, and compatible with KOH etching. The solution to the problem was obtained by a sandwich layer of different materials. The idea was to obtain a material with the same mechanical characteristics as gold, but inert to immobilization, by depositing a thin layer of an inert material on top of the gold. The material needs to have a relative low etch rate in KOH ($< 100 \text{ nm/min}$) and should be able to be deposited at room temperature. The material can then be protected by nickel during the KOH etch, whereafter the nickel can be removed before the measurements are performed.

Tantalum nitride deposited by co-sputtering was found to be a very good candidate. Immobilization test of thiol-modified DNA-oligos were performed which showed a factor of 100 less immobilization on tantalum nitride compared to gold. The etch rate in KOH is less than 10 nm/min and very low in BHF. Figure 5.13 shows a cross-sectional schematic of sandwich layers on the measurement and the reference cantilever. The nickel is removed immediately before performing the measurement in order to keep the gold as clean as possible and thereby increasing the immobilization probability. It is seen that tantalum nitride is also deposited on the measurement cantilever in order to make the two cantilevers as similar as possible.

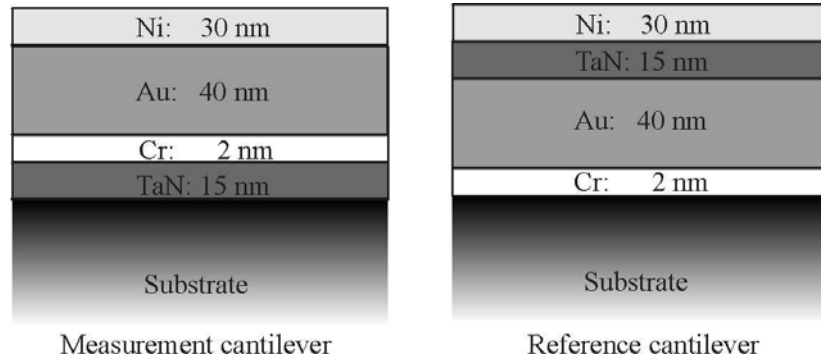


Figure 5.13: Schematic cross-sectional view of the metal sandwich layers on the measurement and the reference cantilever.

5.3.3 SU-8 as the upper part of the wall

As described previously, SU-8 is chosen as the material defining the upper part of the channel wall. Since the SU-8 is lifted off the substrate during KOH etching it has to be deposited after the KOH etch and on the free hanging cantilevers.

The first challenge is to investigate whether the free hanging cantilevers survive the spinning and development of the SU-8. Surprisingly, a test showed that nothing happens to the cantilevers during spinning and structuring of the SU-8. A yield of more than 99 % was observed.

It is necessary to obtain a flat top surface of the SU-8, in order to place a sealing lid on top of the SU-8. Since $50\text{ }\mu\text{m}$ deep channels have been etched into the wafer it is not obvious, that a flat surface is obtained after spinning $50\text{ }\mu\text{m}$ thick SU-8 on top of the wafer. A test was made for investigating the leveling performance of the SU-8 over $50\text{ }\mu\text{m}$ deep channel structures.

$50\text{ }\mu\text{m}$ deep channel structures were etched in KOH using silicon nitride as an etch mask. After baking the wafer at $200\text{ }^{\circ}\text{C}$ for 1 hour, SU-8 1070 [102] was spun onto the wafer at 2000 rpm for 35 sec. This leaves a $39\text{ }\mu\text{m}$ thick SU-8 on a flat wafer. The wafer was then prebaked on a hotplate with a ramping for 15 min to $95\text{ }^{\circ}\text{C}$, where the temperature was kept constant for 15 min. The wafer was subsequently cooled down on the hotplate. After the prebaking, the SU-8 profile was measured by use of a profilometer. A schematic of the profile is seen in figure 5.14a. It can be seen that the SU-8 is not leveled at this point. Therefore, SU-8 was spun unto the wafer once again and prebaked under the same conditions as before. The SU-8 profile is measured once again, the result can be seen as a schematic in 5.14b. It can be seen that the SU-8 profile is now very flat. The change in height over the $50\text{ }\mu\text{m}$ step is reduced to less than $2\text{ }\mu\text{m}$. The SU-8 was hereafter exposed with at dose of 530 mJ/cm^2 , post baked

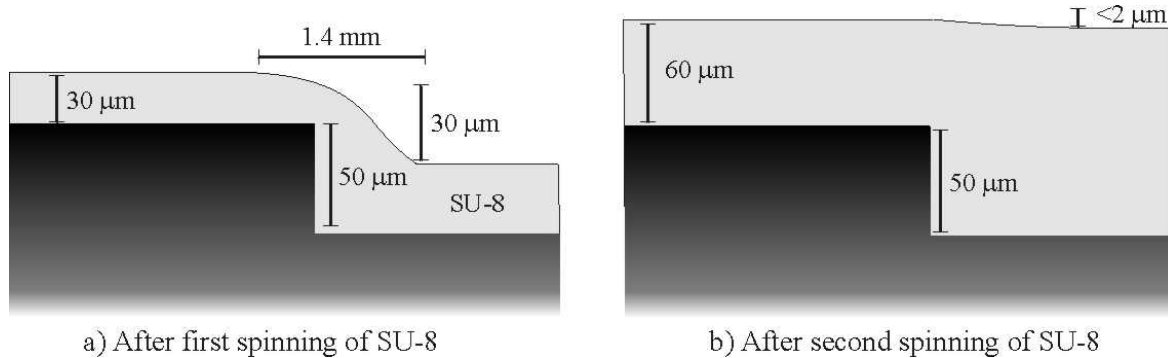


Figure 5.14: Schematic of the SU-8 profile over a $50\text{ }\mu\text{m}$ deep channel. a) shows the profile after 1 spin step, b) after 2 spinning steps. It is seen that the SU-8 is very flat after 2 spinning steps.

at $95\text{ }^{\circ}\text{C}$ for 15 min with a ramping time of 15 min. After development, the SU-8 thickness is measured to $52\text{ }\mu\text{m}$. In figure 5.15 a SEM micrograph shows the leveling of the SU-8 over a step of $50\text{ }\mu\text{m}$. No height variation is observed across the step.

5.4 Summary

In this chapter different process tests have been described. The reason for making these tests was to investigate methods for fabrication of the cantilevers in a channel. Two methods, RIE and KOH etching were investigated for the etching of the channel and for releasing of the cantilevers. A test for RIE of the channel showed that some shadow structures would be left below the cantilevers. It was also found that it would

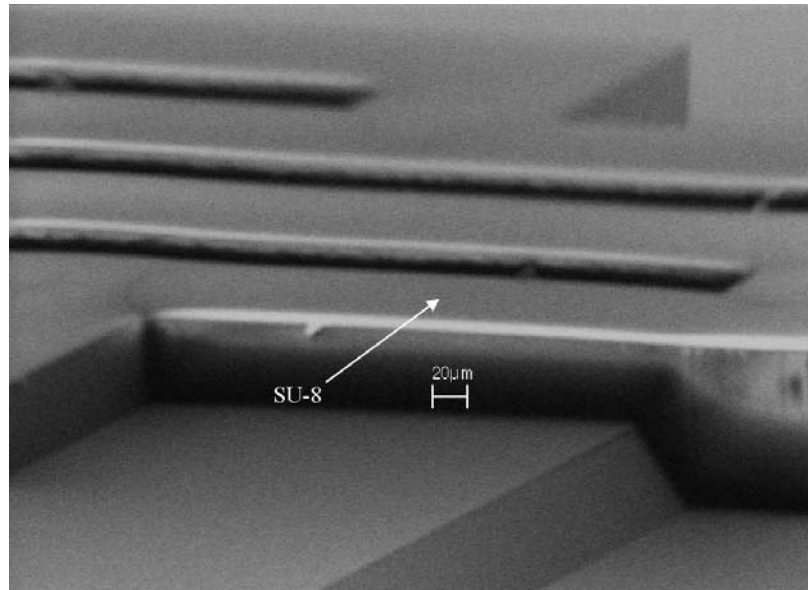


Figure 5.15: The SEM micrograph shows SU-8's leveling profile over a step. A change in height less than $2\text{ }\mu\text{m}$ is observed.

be difficult to mask the cantilever sufficiently during the etching. The KOH etching of the channel did not leave shadow structures below the cantilevers, and no masking of the cantilevers is necessary. Tests showed that SU-8 was lifted during the KOH etching, and the deposition of the SU-8 could first be performed afterwards. Tests showed that the cantilevers did not break during spinning of SU-8 or AZ5214 resist. Only, an ultra-sonic agitated bath will break the cantilevers. A test also showed that SU-8 exhibits very good leveling effects. Due to the above result, it was decided to fabricate the chip with KOH etched channels.

Chapter 6

Fabrication of the chip

In this chapter a detailed fabrication sequence description for a cantilever-based biochemical sensor integrated in a microliquid handling system is presented. Two versions of the fabrication sequence are presented in this chapter. The first version is a proof-of-principle of the fabrication while the second version, includes the enhancements in fabrication and masks design which are observed during the process sequence and characterization of the chip. Version 2 is also presented in appendix B in a short version. The failures are presented here due to the fact that these give an important knowledge for designing a well-functioning chip. The fabrication of version 1, see 6.1.1 and the fabrication of version 2, see 6.1.2 do not differ in most of the steps. The first section of this chapter therefore deal with the fabrication part which is equal for both versions. The fabrication of the version 1 chips has been presented by Thaysen *et al.* [57] at the MEMS 2001 conference.

6.1 Processing of the chip

Double sided polished 4" wafers with a thickness of 350 μm and a resistivity of 1-30 Ωcm (OP51) are used as substrate materials, see figure 6.1a. The wafers are numbered and two wafers are chosen as tests wafers.

A 55 nm thick low stress LPCVD silicon nitride is deposited on the wafer for the definition of the lower part of the cantilever and encapsulation of the cantilever, see figure 6.1b. Since the fabrication of the chip was started before the optimization of the resistor material was finished the silicon piezoresistors are defined in amorphous silicon, which was believed to be the most sensitive polysilicon material. A 150 nm thick amorphous silicon layer is deposited using LPCVD (figure 6.1c). The amorphous silicon is hereafter implanted with boron ions in order to obtain the desired resistivity of the resistors. The doping dose used is $5 \cdot 10^{14} \text{ cm}^{-2}$, implanted with an energy of $E = 30 \text{ keV}$ (figure 6.1d).

The wafer is now ready for the resistor definition. To improve the resist adhesion the wafer is first treated with hexamethyldisilazane (HMDS). A 1.5 μm thick AZ5214E

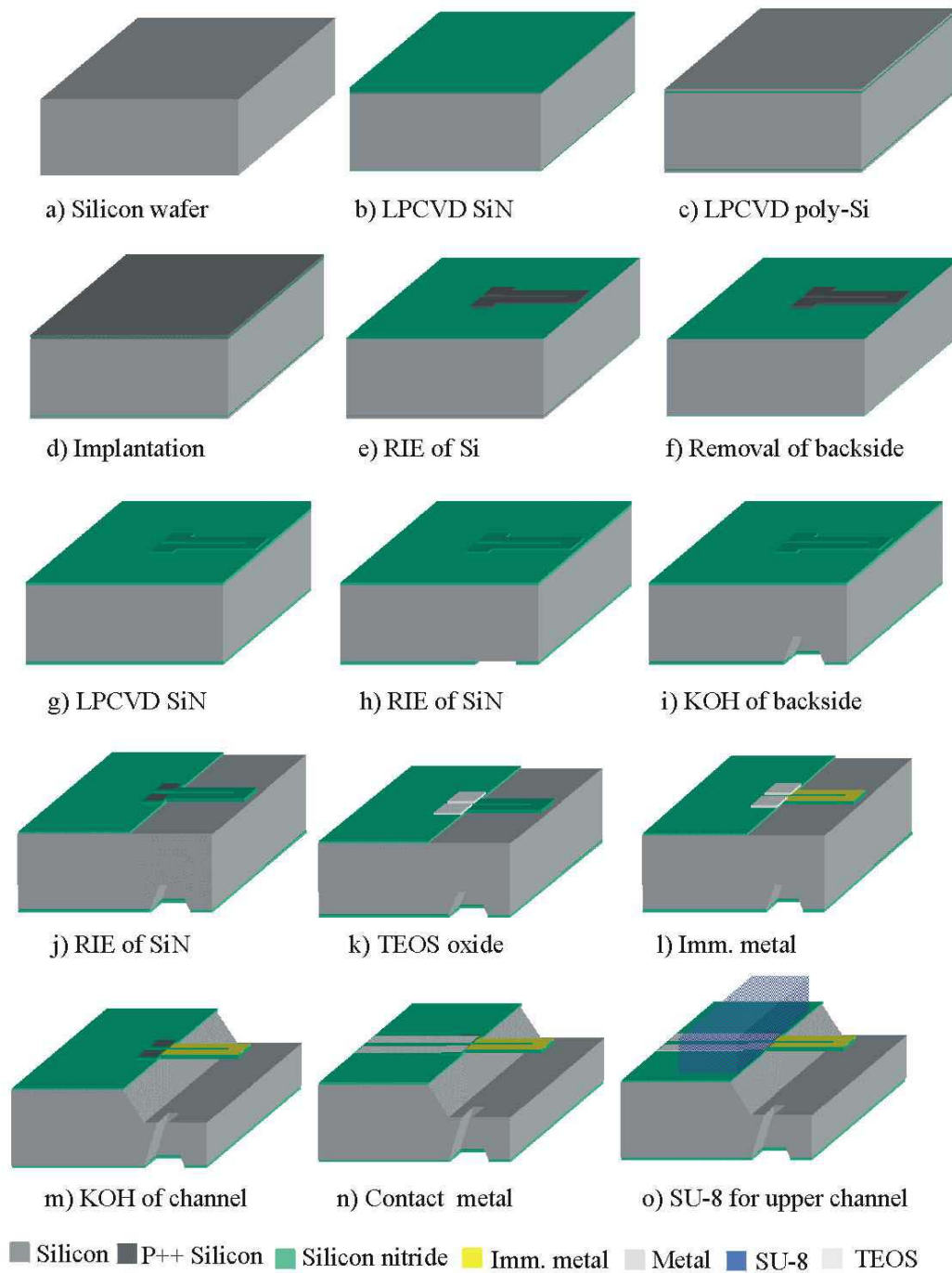


Figure 6.1: The fabrication sequence for making the chip

resist is spun onto the frontside of the wafer. The resistor mask (mask 1) is transferred to the resist by a positive photolithography process and the resist pattern is developed in a sodium hydroxide solution.

The resist pattern is transferred to the underlying amorphous silicon layer by an anisotropic RIE process (6.1e). After inspection of the resistor pattern in the optical microscope the resist pattern is stripped in ultra-sonic assisted acetone for 2 min. The finished resistors are seen in figure 6.2, which shows an optical image of the resistors placed opposite each other.

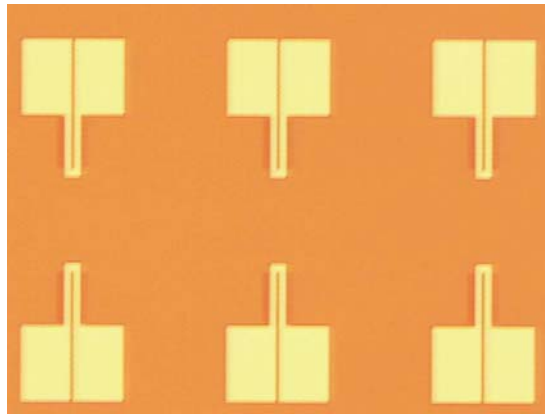


Figure 6.2: *Optical image of resistors after RIE etching*

In order to minimize the resistance of the transversal resistor and the contact pads in the resistor design, these areas are now doped with a boron ion concentration 10 times higher than the resistors. The doping dose is $5 \cdot 10^{15} \text{ cm}^{-2}$, implanted with an energy of $E = 30 \text{ keV}$. After HMDS treatment, a $1.5 \mu\text{m}$ thick resist layer is spun on the wafer and patterned using the implantation mask (mask 2). The resist is hardbaked in an 120°C oven for 25 minutes, in order to withstand the high dose ion-bombarding. Figure 6.3 shows an optical image of the resistor with the implantation mask. The areas protected by the resist define the stress sensitive resistor. After the implantation

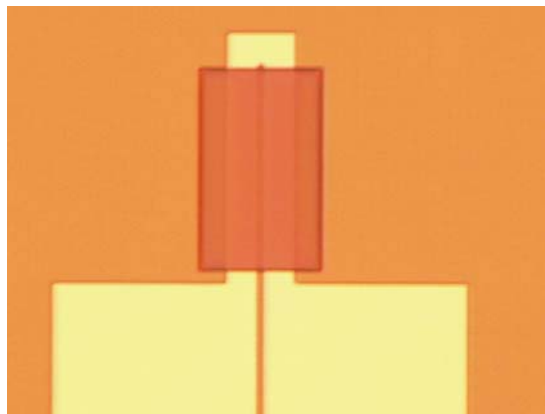


Figure 6.3: *Optical image of the resistors with the implantation mask. The non-mask area is highly doped for minimizing the resistance of these areas.*

the resist mask is stripped by ashing in an oxygen plasma for 30 min. The result is shown in figure 6.4, where a color change indicates the placement of the removed implantation mask. Next, the amorphous silicon layer is removed on the backside of

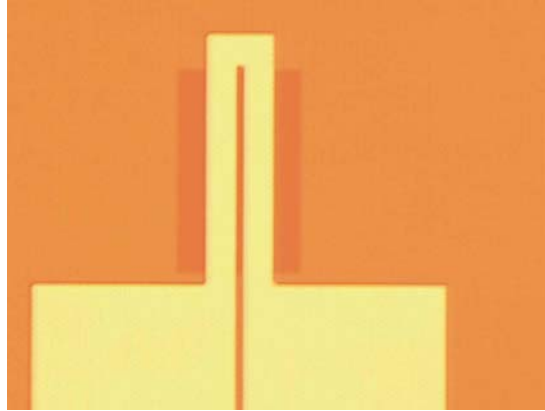


Figure 6.4: Optical image after stripping of implantation mask. The color change indicates the previously masked area.

the wafer. This is done since the in/outlet is etched from the backside in KOH using silicon nitride as an etch mask. If not removed, the amorphous silicon layer will be etched during the KOH etching and in a worst case scenario destroy the etch mask. The front side is protected by a $1.5\ \mu\text{m}$ thick resist. The wafer is etched in a polysilicon wet etching bath for 3 min, whereafter the resist is stripped in acetone, see figure 6.1f.

In order to encapsulate the resistor completely in silicon nitride a new LPCVD low stress silicon nitride layer is deposited on top of the wafer. The wafer is cleaned in an RCA cleaning step whereafter a 280 nm thick silicon nitride layer is deposited, see figure 6.1g.

The in/outlets can now be defined from the backside of the wafer. After a treatment with HMDS, a $1.5\ \mu\text{m}$ thick resist is spun on the backside of the wafer. Using photolithography, the in/outlet mask (mask 3) is transferred to the resist. The silicon nitride is then etched using RIE, with a selective silicon nitride to silicon etch process. After optical inspection, the resist is stripped in acetone, see figure 6.1h.

The in/outlet holes are now etched using KOH at $80\ ^\circ\text{C}$. The etch is stopped after 200 minutes leaving $90\ \mu\text{m}$ thick membranes in the in/outlet holes, see figure 6.1i.

It is now possible to define the channel in the silicon nitride. Since the cantilevers also are defined in the silicon nitride, and the contact hole to the resistor in the upper silicon nitride layer, all these are parts are defined in the same mask step. After a HMDS treatment an $1.5\ \mu\text{m}$ thick resist is spun onto the wafer, mask 4 is transferred to the resist using photolithography. The patterns are etched using an RIE which exhibits a selectivity between silicon nitride and silicon such that the amorphous silicon material

in the contact holes is not etched during the etching of the lower nitride layer, see figure 6.1j. After the RIE the resist is stripped using acetone and the wafer is inspected in an optical microscope. Figure 6.5 shows an optical image of the wafer after the definition of the channel, cantilever and contact hole.

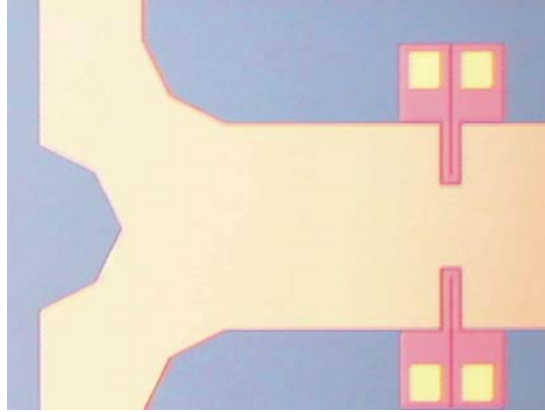


Figure 6.5: *The optical image shows the channel and the cantilever after RIE of the silicon nitride. Note the opening in the resistor pads for the electrical connection.*

As described in chapter 5, the contact holes need to be protected during the KOH etching of the channel. The contact holes are protected by a TEOS oxide during the 70 minutes long KOH etching of the channel. The TEOS oxide has an etch rate of 5 nm/min in 70 °C hot KOH. In order to make sure that the TEOS oxide sustains the later KOH etching, a 7100 Å thick TEOS oxide is deposited on the wafer after a RCA cleaning. Hereafter, a 1.5 μm thick resist is spun on the front side of the wafer and patterning with the TEOS mask (mask 5) using photolithography. The TEOS oxide is etched in BHF for 10 minutes. The etch rate of the TEOS oxide in BHF is 300 nm/min, but the TEOS in the in/outlet holes on the back side is more difficult to etch due to surface tensions of the BHF. Nevertheless, the TEOS oxide was etched away, also in the in/outlet holes after 10 minutes. The resist is then stripped in acetone. The actual fabrication step is shown in figure 6.1k.

An optical image of the wafer, after the patterning of the TEOS oxide is shown in figure 6.6. It can be seen that the TEOS oxide protects the contact holes, but also defines the corner compensation in the channel junction. The corner compensations are designed such that the KOH etched channel will follow the channel, defined in the silicon nitride.

6.1.1 Fabrication of version 1

At this point, most of the wafers were left without further processing. This was done in order to test some of the inventive steps on the real design and from the result conclude whether some of the design or the fabrication steps, need to be changed in

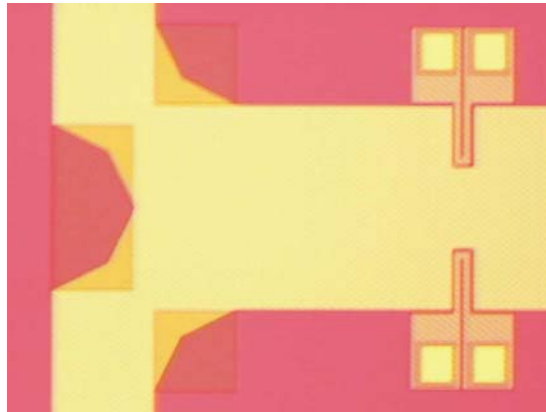


Figure 6.6: *The optical image shows the wafer after the patterning of the TEOS oxide. The TEOS oxide is both used as contact hole protection and as corner compensation for the later KOH etching of the channel.*

order to make a well function chip.

A gold layer is required on the measurement cantilever for the thiol immobilization. After at HMDS treatment, an $1.5\ \mu\text{m}$ thick resist is spun on the wafer. By photolithography, the immobilization metal mask (mask 7) is transferred to the resist. A chromium/gold layer with thicknesses of 2 nm and 40 nm respectively, is deposited onto the wafer using e-beam evaporation. The metal is lifted using ultra sonic agitated acetone leaving the metal only on the measurement cantilevers, see figure 6.1l. In version 1, no metal is deposited onto the reference cantilever.

After the metal deposition on the measurement cantilever, the channel is etched in $70\ ^\circ\text{C}$ hot KOH for 70 minutes, leaving a $55\ \mu\text{m}$ deep channel with free hanging cantilevers. The KOH etching also etches away the $90\ \mu\text{m}$ thick membrane in the in/outlet holes, see figure 6.1m. In figure 6.7 an optical image shows a close-up of a chip at the channel junction. It can be seen that only one of the cantilevers have gold on the top surface. It is also observed that corner compensation has resulted in a KOH channel following the silicon nitride mask opening without serious undercutting.

The TEOS oxide at the contact holes and for the corner compensation is etched away in BHF, and a titanium/aluminium metal layer is deposited by e-beam evaporation with thickness of 10 nm and 500 nm respectively. The metal layer is patterned and used for the electrical contacts, as described in chapter 5. A recipe for $4.2\ \mu\text{m}$ thick resist is used for the coating of the structured wafer. After exposing the resist through the electrical contact mask (mask 8), the pattern is developed in a sodium hydroxide solution. The resist is hardbaked in an furnace at $120\ ^\circ\text{C}$ in 30 minutes whereafter the aluminum is etched in phosphorus acid for 5 minutes, see figure 6.1n.

The resist is stripped in an oxygen plasma in the asher, and the result is shown in

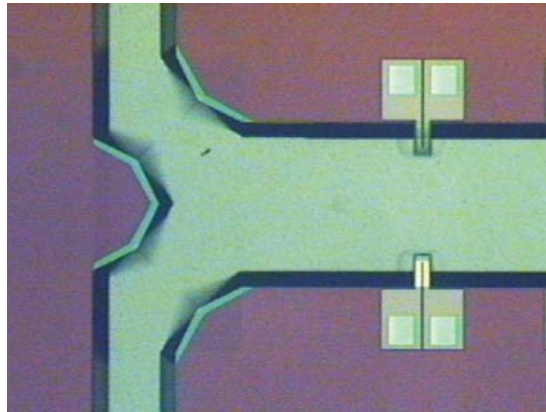


Figure 6.7: *Optical image of the channel junction after the KOH etching of the channel.*

figure 6.8. Two optical images are shown in the figure. The left optical image shows the metal wires connected to the resistor through the contact pads. Note that all the metal is removed in the channel. In the right optical image in figure 6.8, it can be seen that the metal has not been removed completely in the channel. This is due to an insufficient exposing dose, which has resulted in under-exposure of the relative thick resist in the channel. Even though the same procedure was used as described in chapter 5, the fact that the wafer has in/outlet holes resulted in another resist distribution on the wafer as on the test wafers. This resulted in a thicker resist in the channel at the center of the wafer. It was not possible to expose the resist with an even higher energy, since the line width of the metal wires would decrease severely. It can be seen that the metal on the lower contact pads are already damaged due to over-exposure.

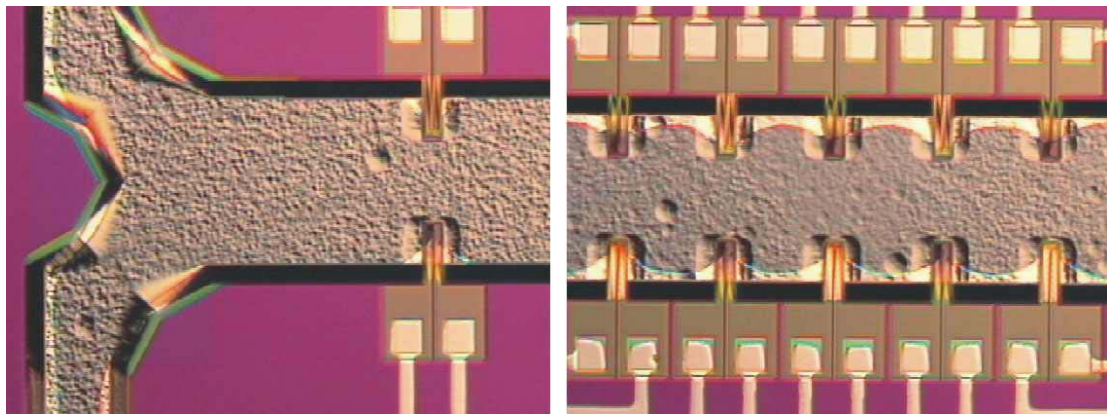


Figure 6.8: *Two optical images of the cantilevers in the channel after the electrical connection definition. The left picture shows the channel junction. No metal is observed in the channel. It is seen in the right picture that the metal is not removed completely in the channel.*

The wafer is now ready for the definition of the upper-part of the channel, which is fabricated in SU-8. The wafer is ashed in an oxygen plasma for 30 minutes in order to obtain better adhesion of the SU-8 to the substrate. SU-8 1070 is spun on the wafer with a rotation speed of 4000 rpm. Hereafter the wafer rests for 60 minutes in order to reflow the SU-8. The wafer is baked on a hotplate at 90°C in 55 minutes. The wafer is elevated 1 mm due to the SU-8 on the backside, which is obtained due to in/outlet holes. The hotplate is ramped from room temperature to 90°C in 15 minutes, and cooled down to room temperature during 60 minutes.

SU-8 is once again spun onto wafer, this time with a rotation speed of 3000 rpm. The pre-baking procedure is repeated. The SU-8 is exposed in order to transfer the SU-8 mask (mask 9) to the SU-8. The wafer is hereafter postbaked at 95°C in 15 minutes, with a 15 minutes ramping. Finally, the SU-8 is developed in PGMEA for 14 minutes, yielding the finished chips, see figure 6.10.

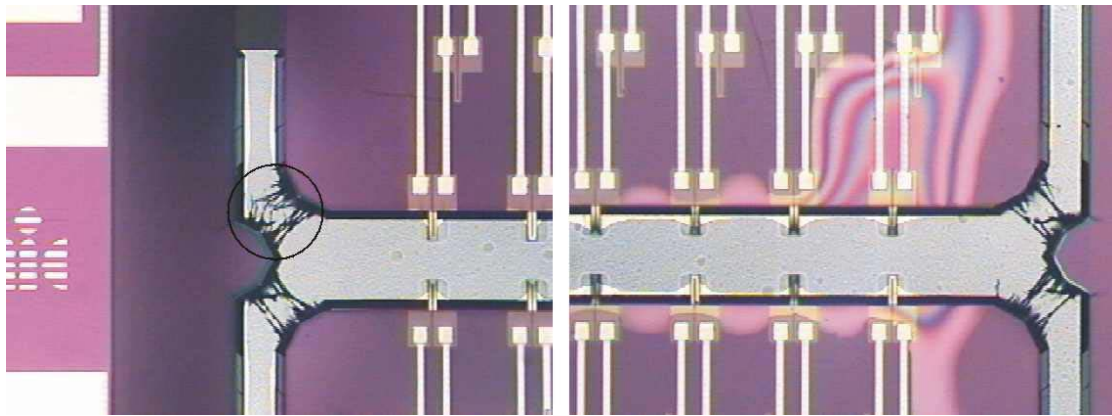


Figure 6.9: Two optical images of the channel after the deposition of SU-8. The left image shows that SU-8 fibers are sticking out in the channel. The right image shows an example of non-sticking SU-8. The non-sticking is observed as a color change in the SU-8.

In figure 6.9 two optical images of the wafer are shown after the SU-8 upper side wall definition. The left image shows the channel junction. The color change at the substrate indicates the transition between the SU-8 and the substrate. It can be seen that some fiber-like structures are sticking into the channel from the channel junction. The reason why these fibers are obtained is probably due to the SU-8 mask has been designed too small. When the SU-8 is exposed through a too small mask, the light will hit the (111)-plane side wall in the KOH etched channel. The side wall will act like a mirror and then exposing the SU-8 in the channel, which will then polymerize, see figure 6.10. The fibers can also be observed in the SEM micrograph in figure 6.11, which support the explanation. It is observed that the fibers points downwards with an angle that corresponds to the KOH etched channel side walls. The right image in

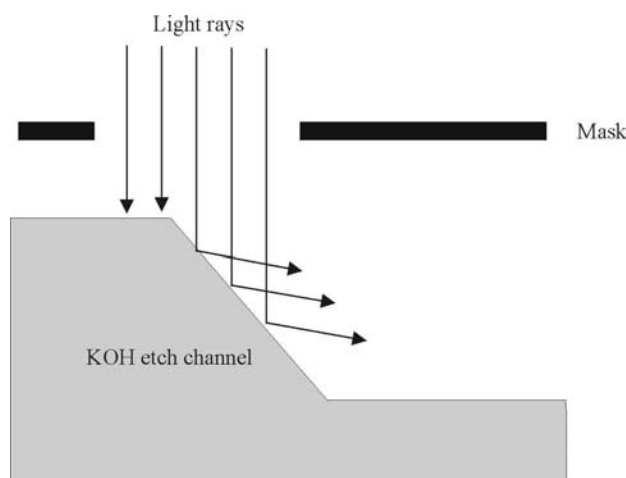


Figure 6.10: *The schematic shows why SU-8 fibers are obtained in the channel due to a too small mask*

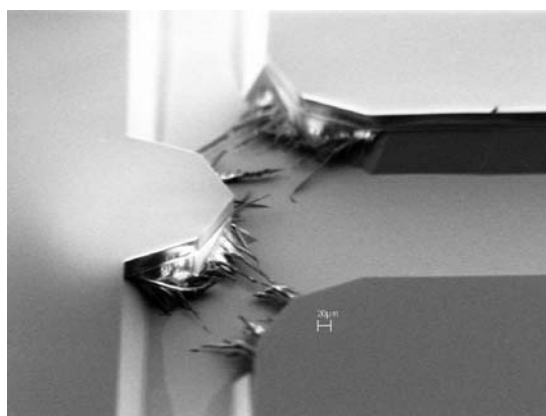


Figure 6.11: *The SEM micrograph supports the explanation why the SU-8 fibers are obtained in the channel*

figure 6.9 is a chip where the SU-8 does not adhere properly to the substrate. The non-adhesion is visualized as a color change in the SU-8.

Further characterization of the chip is given in the next chapter. But it can be revealed, that it was difficult to immobilize molecules on the gold on the cantilevers. The reason for this is probably due to the rough treatment of the gold before using it: The oxygen plasma ashing for removing resist and cleaning the substrate made the gold surface very rough. The KOH etching of the silicon might have polluted or even damaged the gold surface, and SU-8 residues might still adhere to the gold. Finally, the gold is polluted when left in atmospheric air non-protected. These problems were solved in version 2 of the chip.

6.1.2 Fabrication of version 2

Due to the problems observed when fabricating the first version of the chip, a second version of the chip was fabricated. The design of the electrical connection wires was changed such that the width of the wires were increased in order to increase the over-exposure time and thereby remove the metal in the channel completely. The SU-8 mask was expanded in order to prevent the SU-8 fibers in the channel. It was also decided to deposit the two sandwich metal layers on the measurement cantilever and the reference cantilever, respectively. As described in chapter 5 this is done in order to obtain two nearly similar cantilever performances. Nickel is deposited on top of the metal layers as protection during the rest of the processing and before using the chip. Finally, the oxygen plasma ashing of the chip is prevented, and instead a dehydration in a 250 °C furnace is used before the deposition of the SU-8.

The fabrication of the second chip version is not described in details since the fabrication sequence resembles very much the first version fabrication sequence. The metal layers deposited on the measurement cantilever are tantalum nitride, chromium, gold and nickel with thickness of 15 nm, 2 nm, 40 nm and 30 nm, respectively. While the metal sandwich layer deposited on the reference cantilever are chromium, gold, tantalum nitride and nickel with the thickness 2 nm, 40 nm, 150 nm and 30 nm respectively. Figure 6.12 shows a reference cantilever and a measurement cantilever before the KOH etching. Both cantilevers have the same color due to the nickel protection layer. After

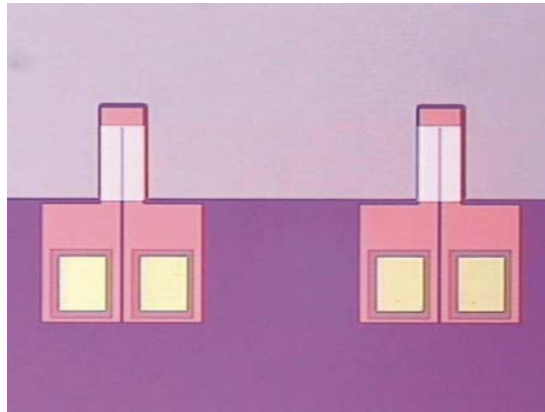


Figure 6.12: *An optical image of a reference and a measurement cantilever before KOH etching. The reason for the same color of the metal layer is due to the nickel protection layer.*

the electrical connection definition and the patterning of the SU-8 for the upper side wall, chips without metal in the channel and SU-8 fibers were realized. The SU-8 was also changed to SU-8 XP-50 from MicroChem Corp. [103] in the second chip version, due to reproducibility problems with the SU-8 1070 from Sotec Microsystems. The spinning and baking procedures were also changed in order to obtain a better SU-8 with respect to adhesion and planarization. Tests showed that spinning two times 2500

rpm directly after each other without any baking step in between yielded the same result with respect to planarization as the procedure mentioned in chapter 6. The SU-8 is then pre-baked at 70 °C in 1 hour. After exposing the SU-8, a 70 °C postbaking for 1 hour is performed. After development, the SU-8 is hardbaked at either 95 °C or 120 °C.

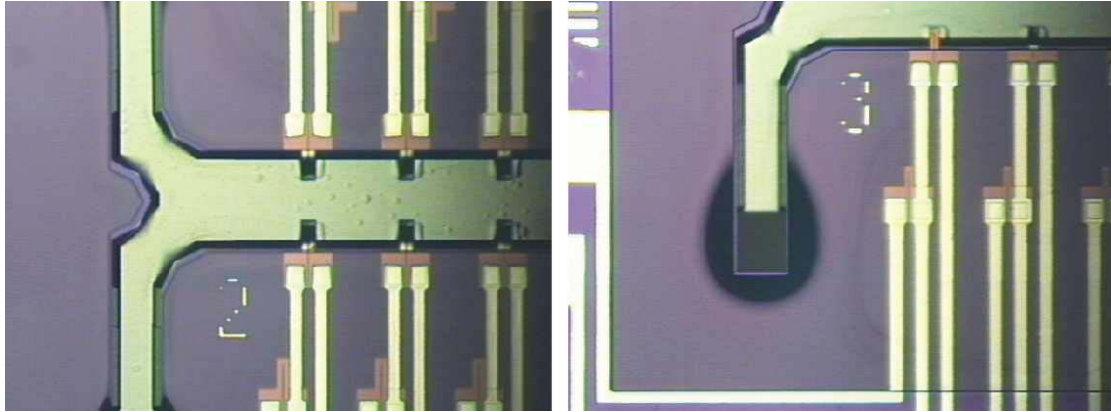


Figure 6.13: An optical image of a chip after the SU-8 patterning. It is seen from the image that no metal and SU-8 fibers are observed in the channel.

In figure 6.13, two optical images of the realized second version of the chip is seen .It can be seen on the right picture that the SU-8 is much darker around the inlet holes. This phenomenon is actually due to the fact the SU-8 height decreases around the inlet holes. The height variation is obtained due the prebaking of the SU-8. The hot SU-8 is much more viscous than the cold SU-8. Therefore, the SU-8 tends to flow into

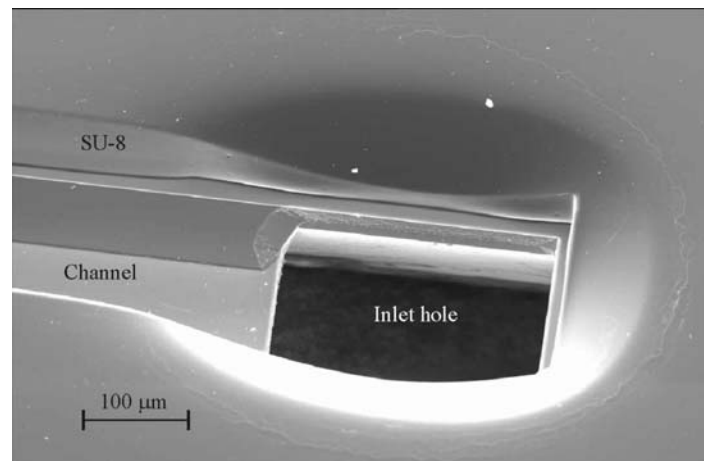


Figure 6.14: The SEM micrograph shows the thickness variation of the SU-8 around an inlet hole.

the inlet hole, yielding the thickness variations. The SEM micrograph in figure 6.14

visualizes the phenomenon. Since the thickness variation is only observed very close to the inlet holes, it does not complicate the sealing of the channel by a lid.

In figure 6.15 a SEM micrograph of a chip design 3 from fabrication version 2 is shown. It can be seen that no SU-8 fibers are observed in the channel. On the channel corners of the KOH etched channel, the etch profile due to the crystal plane dependent etch rate can also be seen.

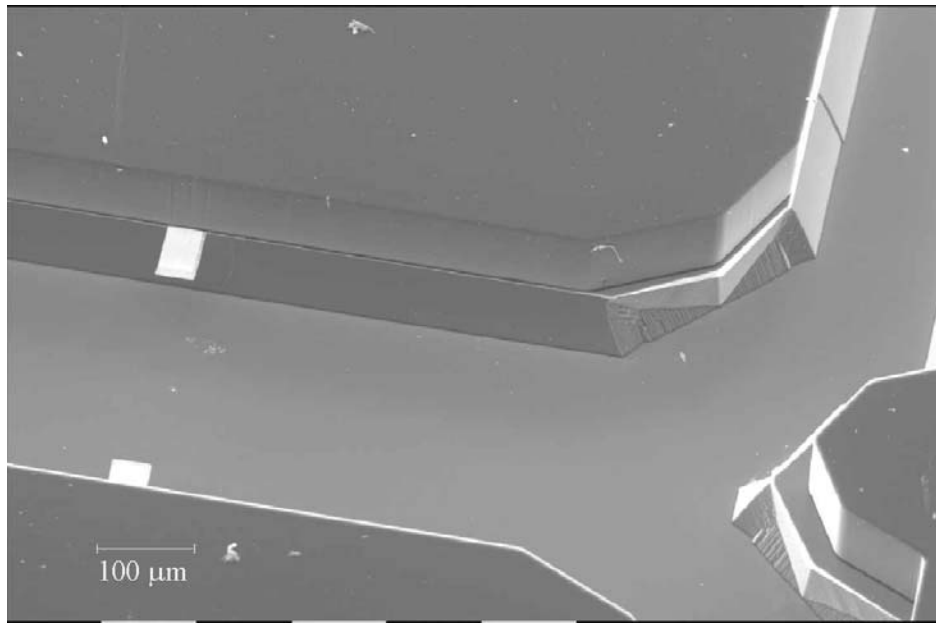


Figure 6.15: *An optical image of a chip after the SU-8 patterning. It is seen from the image that no metal and SU-8 fibers are observed in the channel.*

From the above optical images and SEM micrograph it can be concluded that the fabrication of the version 2 chips was successfully realized. In the next chapter the characterization of the chips is discussed.

6.2 Summary

The fabrication of the chips was described in this chapter. A first fabrication version of the chips was made as a proof-of-principle. The fabrication was described step by step, and is also documented in appendix B. The fabrication consists of 53 fabrication steps and 9 masks. It was found that some SU-8 fibers were sticking out in the channel due to a design mistake. A fabrication of an enhanced version was realized. A sandwich layer matching the mechanical properties of the sandwich layer on the measurement cantilever was deposited on the reference cantilever in order to optimize the performance of the *on-chip* filter.

Chapter 7

Characterization

In this chapter the characterization of the chip is described. The characterization is performed in order to investigate whether the chip performs as expected from the theory and the design. A visual inspection is performed by optical microscopy and SEM for both version 1 and 2. Hereafter, the sensitivity of the cantilevers is measured and the gauge factor is calculated. In order to determine the lowest detectable surface stress change, noise measurements are performed and evaluated. Finally, the thermal stability of chips from version 1 is compared to chips from version 2 in order to investigate whether the *on*-chip filter has been enhanced due to the materials on the reference cantilever.

7.1 Visual inspection

The adhesion of the SU-8 is very important in order to obtain a well functioning chip. A chip with adhesion failure used in a measurement, malfunctions since the liquid flowing in the channel gets in contact with the electrical connections to the resistor. When this happens the aluminum is etched due to a catalytic reaction. Even for deionized water the etching of the aluminum happens within seconds.

No quantitative test of the SU-8 adhesion to the substrate has been developed and the adhesion failures have therefore only been determined by means of optical microscopy investigations. Nevertheless, this method has turned out to be a very easy and reliable way to determine the adhesion failure. As already shown in figure 6.9 the adhesion failure is visualized as a change in color. In version 1 about 40 % of the chips turned out to have SU-8 adhesion failure. The low yield origins in the mask design. During the optical inspection it was observed that the SU-8 adhesion failure always took place on the same side of the chip. The chips were therefore investigated in the SEM in order to find an explanation. Figure 7.1 shows a close up of the channel. The white arrow indicates where the SU-8 pattern stops. It can be seen that the SU-8 side wall has a small over-hang with respect to the silicon channel side wall. The reason for this is that the SU-8 mask was designed too big. Due to a mis-alignment on the order of a couple of micrometers, the over-hang is only observed on one side of the channel. The

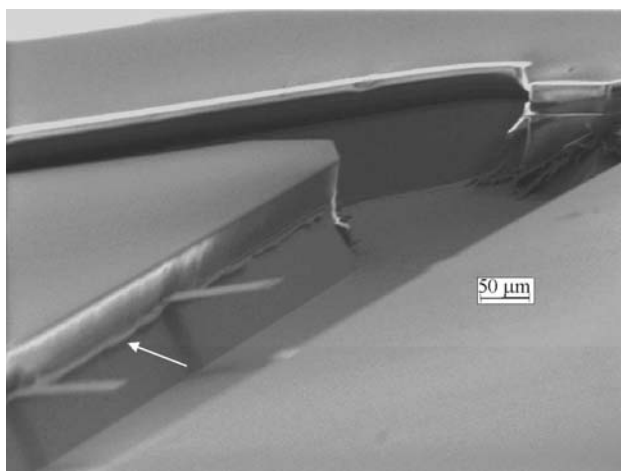


Figure 7.1: SEM micrograph of the channel. Due to the small over-hang of the SU-8 channel side wall with respect to the silicon channel side wall indicated with the white arrow, an adhesion failure of the SU-8 was observed.

adhesion problem was only observed on the same side as the SU-8 over-hang, and it was therefore concluded that the SU-8 over-hang probably leads to the SU-8 adhesion failure.

The SU-8 mask design was changed in order to take care of this problem in version 2, and the chips turned out to have a very high yield on the SU-8 adhesion, even better than 99 %. Figure 7.2 shows that no over-hang is observed in version 2.

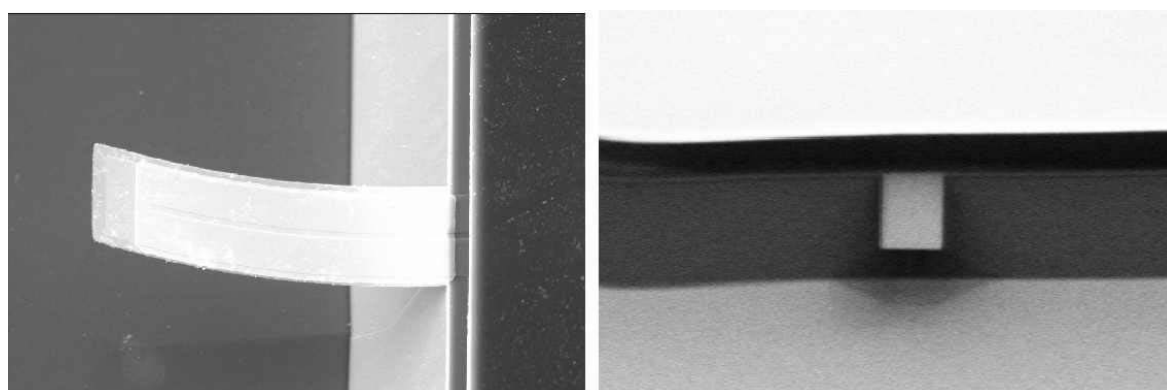


Figure 7.2: The SEM micrograph shows that no over-hang is observed in version 2.

Figure 7.3 shows two SEM micrographs of the chip A from version 1. The left micrograph shows the whole chip. The electrical connection wires can be seen. From this micrograph the SU-8 side wall is also very distinct. The right micrograph shows a close-up of the channel. In the right SEM micrograph of figure 7.3 and in figure 7.1 it

is seen that the cantilevers are straight and placed in the middle of the side wall.

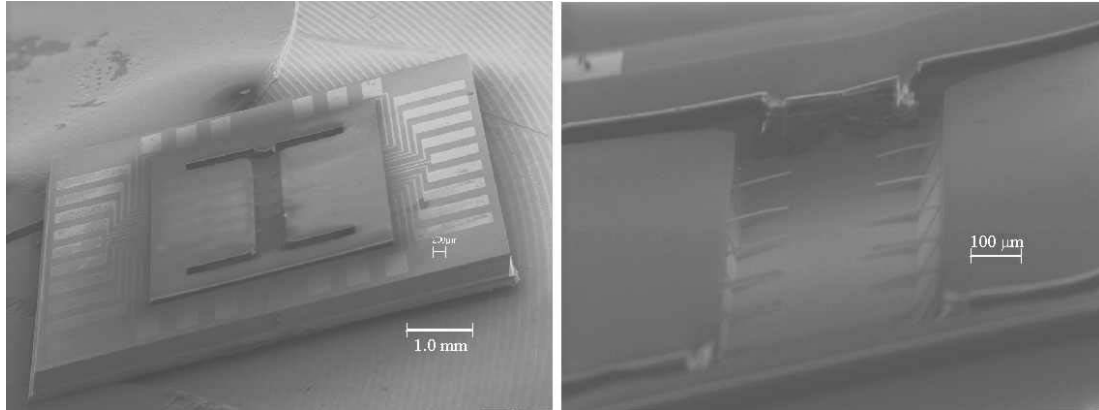


Figure 7.3: Two SEM micrographs of the chip. The left shows the whole chip, while the right is a close-up of the channel.

The chips are released from the wafer by dicing using a saw with a very fine blade. For version 1 none of the cantilevers broke during the dicing, but unfortunately all the cantilevers, except the short ones in chip design C, broke during the dicing of version 2. The reason for this is still not clear, but it is believed that the bending of the cantilevers, due to the high stress level in the nickel film, has an influence on the phenomenon. In figure 7.4 two SEM micrographs of chips with short cantilevers are shown from version 1 and 2. It can be seen that the cantilever from version 2 is much more bend compared to the cantilevers in version 1.

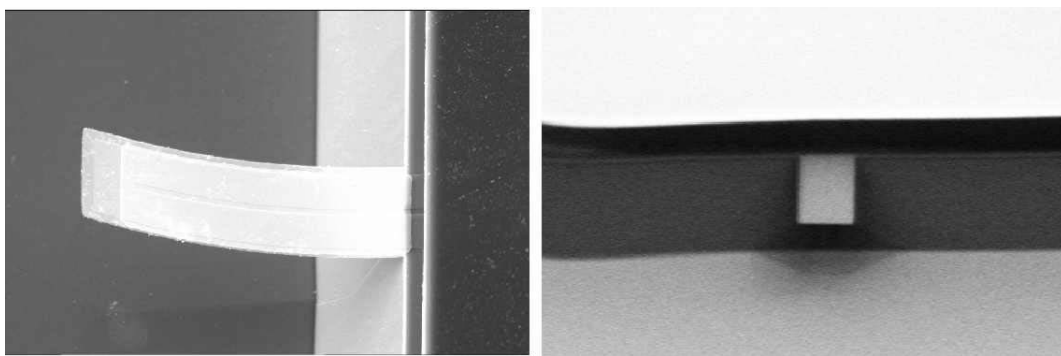


Figure 7.4: SEM micrographs of cantilevers from two different chips. The left chip is from version 2. It can be seen that this cantilever is very bended due to the nickel layer, when compared to a cantilever from version 1 (right).

A probable explanation is described here: When the wafer was diced, water was poured onto the wafer. The water forces the cantilever to bend such that the end of the

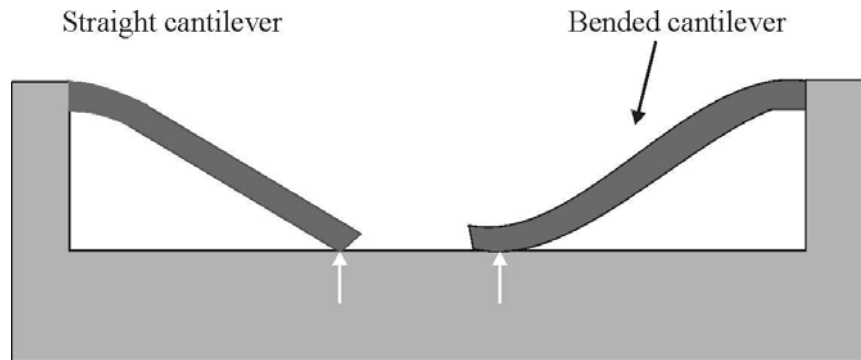


Figure 7.5: The schematic shows the contact area (white arrows) to the channel floor for a straight and a bended cantilever forced down by water pressure.



Figure 7.6: SEM micrograph of a broken cantilever. It can be seen that it is in contact with the channel floor.

cantilever is in contact with the channel floor. During the dicing a lot of vibrations were obtained. Since the bended cantilevers have a larger contact area to the channel floor than the straight ones, see figure 7.5 more vibrational energy was transferred from the channel floor to the cantilevers and eventually broke them, see figure 7.6.

7.2 Actual dimensions and resistivity

The dimensions of the thin film layers found during processing differs from the expected thicknesses presented in table 4.1. These differences have an influence on the performance of the cantilever and the actual thin film thicknesses are therefore presented in table 7.1.

It can be seen that the total thickness of the cantilever, without tantalum nitride is 530 nm.

The resistance of the piezoresistors is measured for the three different resistor volumes.

Thin film	$h[nm]$
<i>Au</i>	40
<i>(TaN)</i>	15
<i>Si₃N₄</i>	280
<i>Si p⁺⁺</i>	155
<i>Si₃N₄</i>	55

Table 7.1: The actual thicknesses of the thin films found during the fabrication. The tantalum nitride is only present on cantilevers in version 2.

The data is plotted in figure 7.7 where the resistance is plotted as a function of $\frac{2\lambda}{h_r w_r}$. The resistivity can now be found from the slope of the straight line to $\rho = 2.8 \cdot 10^{-2} \Omega cm$.

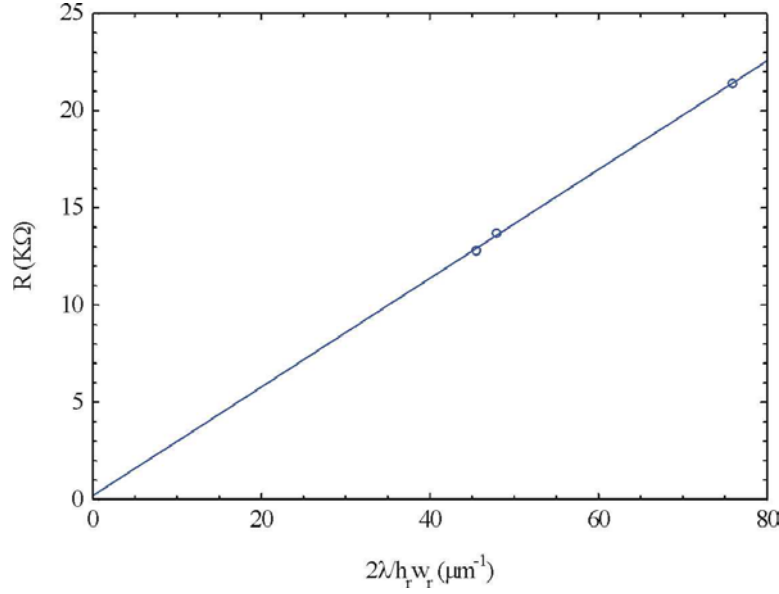


Figure 7.7: Resistance as a function of $\frac{2\lambda}{h_r w_r}$. The slope is the resistivity ρ and the intersection with the y -axis is the resistance of the transverse part of the resistor.

The resistance of the transverse part of the resistor is found as the intersection with the y -axis, and is approximately 190 Ω . Since the resistors have resistance in the order of 20 k Ω , the transverse part amounts to about 1 % of the total resistance. This was also expected since the transverse resistor part has been doped with a 10 times higher dose than the rest of the resistor.

7.3 Sensitivity

In order to investigate the performance of the cantilevers, the end-point deflection sensitivity is measured. It is of course more convenient to measure the surface stress sensitivity directly, but unfortunately, no measurement setup has been available for this. A method for measuring the surface stress sensitivity directly could for example

be to etch a metal with a known build in stress from the sensor surface . The signal obtained from the piezoresistor during the etching could then be converted to a measure of the surface stress sensitivity.

As described in chapter 3, the gauge factor is calculated from the end-point deflection sensitivity graph and then converted into a number for the surface stress sensitivity. Figure 7.8 shows the relative change in resistance as a function of end-point deflection of the cantilever. The graph shows a curve for a cantilever from design 1 and 2. By comparing with the theoretical sensitivities found in table 4.3 it is seen that these are in good agreement with the measured end-point sensitivities. Using the thin film

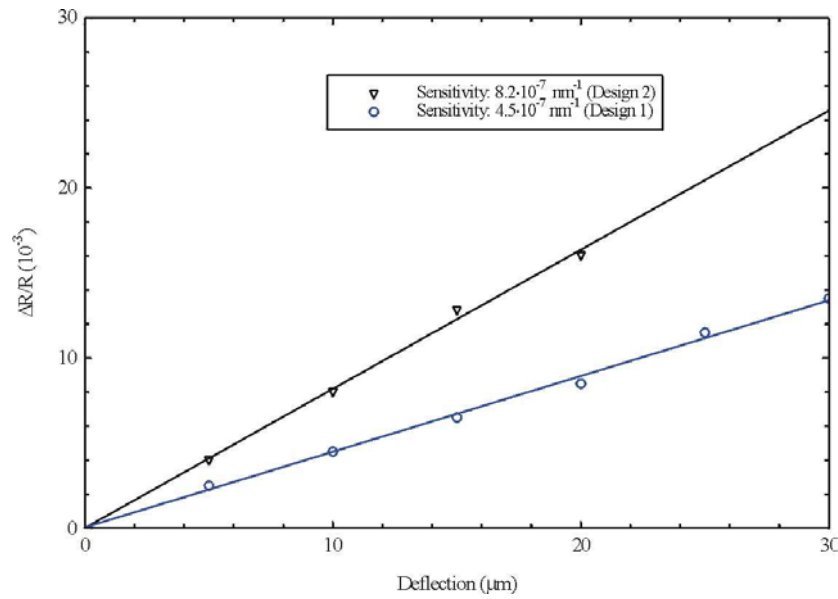


Figure 7.8: The graph shows the relative change in resistance as a function of end-point deflection for cantilevers from design 1 and 2.

thicknesses presented in table 7.1 the gauge factor is calculated by using expression 2.2-5. The gauge factor is calculated to $K = 30$, which is conformity with the gauge factor ($K = 32$) found for low annealed low doped amorphous silicon in table 3.4. The difference in gauge factors might be due to different annealing conditions. During fabrication of version 1 and 2, the resistors were only annealed at $T = 835$ °C, while the chips made for the gauge factor characterization in chapter 3 were annealed at $T = 950$ °C

7.4 Electrical noise

The electrical noise was measured in order to determine the minimum detectable surface stress change. The noise was measured in a setup described in chapter 3.2.2 on chip design A. The measurements were performed with supply voltages of 0 V, 1.5 V, 3.0 V, 6.0 V and 9.0 V and the results are presented in figure 7.9. It is seen from

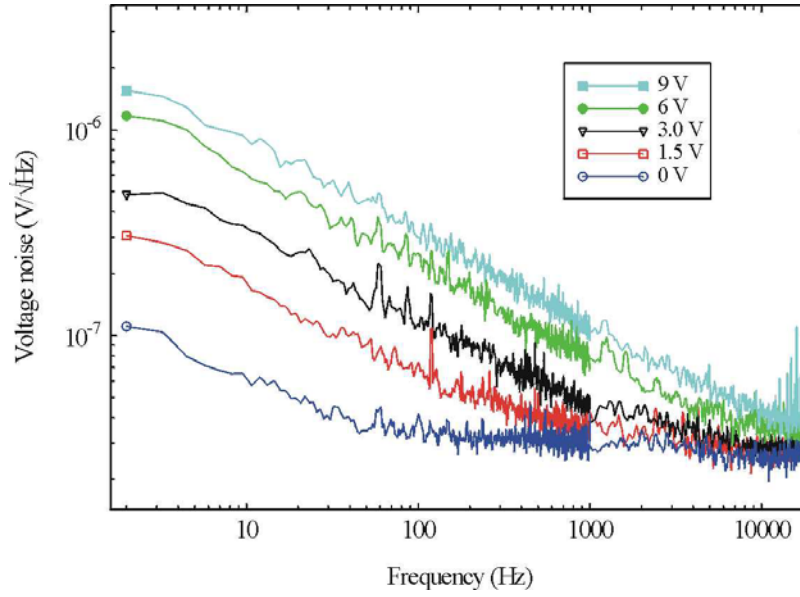


Figure 7.9: Voltage noise as a function of frequency for different supply voltage.

the figure that the trend in the noise as a function of supply voltages corresponds well with the results observed in chapter 3. In order to measure the α -factor from the noise curves by the same method as in chapter 3, resistors with constant l/w -ratio as a function of l are required, see equation 3.2-3. Since the design does not include such resistors, another approach for measuring the noise is used.

The expression for the $1/f$ -noise in equation 2.4-4 is

$$S_{Hf} = \frac{\alpha V_{sup}^2}{fN}$$

This equation can be rewritten to

$$\sqrt{S_{Hf}f} = \sqrt{\frac{\alpha}{N}} V_{sup} \quad (7.4-2)$$

From this expression it can be seen that $\sqrt{\frac{\alpha}{N}}$ can be found as the slope when plotting $\sqrt{S_{Hf}f}$ as a function of V_{sup} . α can then be determined when the total number of carriers in the resistor is known. In figure 7.10 the plot of $\sqrt{S_{Hf}f}$ as a function of V_{sup} is presented. The slope is calculated to $\sqrt{\frac{\alpha}{N}} = 3.1 \cdot 10^{-7}$. The calculation is performed for a design 1 cantilever. Since the carriers in the transverse resistor part can be neglected the total number of carriers can be calculated to $N = 1.7 \cdot 10^{10}$. The α -factor is then calculated to $\alpha = 1.6 \cdot 10^{-3}$. In comparison the α -factor found for low doped low annealed amorphous silicon was $\alpha = 1.3 \cdot 10^{-3}$. Since the annealing conditions are changed and the calculation of the α -factor differs, the two results are in good agreement.

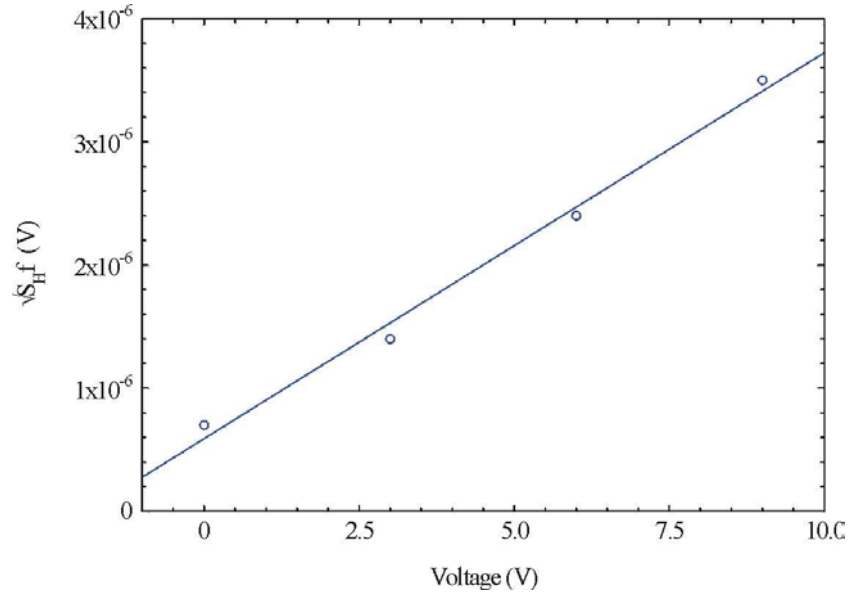


Figure 7.10: The graph shows a plot of $\sqrt{S_H f}$ as a function of V_{sup} . The α -factor can be determined from the slope, when the total number of carriers in the resistor is known.

Design	$\frac{\Delta R}{R}/\sigma_s$ [m/N]	$\sigma_{s,min}$ [N/m]	k [N/m]	f_{res} [kHz]	$\frac{\Delta R}{R}/z$ [nm ⁻¹]
1	$1.6 \cdot 10^{-4}$	$1.8 \cdot 10^{-2}$	0.17	39	$-0.45 \cdot 10^{-6}$
2	$1.6 \cdot 10^{-4}$	$2.3 \cdot 10^{-2}$	0.55	85	$-0.90 \cdot 10^{-6}$
3	$1.6 \cdot 10^{-4}$	$1.4 \cdot 10^{-2}$	0.25	39	$-0.45 \cdot 10^{-6}$

Table 7.2: Actual performance of the cantilever designs. The gauge factor and α factor are measured to $K = 30$ and $\alpha = 1.6 \cdot 10^{-3}$. The supply voltage is $V_{sup}=5$ V and the bandwidth is $\Delta f=1$ Hz - 51 Hz.

7.5 Actual performance

Based on characterization of the electrical resistance, the thin film thicknesses, the gauge factor and the noise it is now possible to list the performance of the different cantilever designs. The data is presented in table 7.2. By comparing the actual performance with the expected performance given in table 4.3 it can be seen that the change in surface stress sensitivity is about 15 % less than expected, and the minimum detectable surface stress about 30 % less than expected. This is due to differences in gauge factor, α -value and cantilever material thicknesses. Still, it can be concluded from the characterization that the chip performance is in good agreement with the expected values.

<i>On-chip filter</i>	Measurement cantilever	Reference cantilever
a	Au	SiN
b	Au	Au
c	Au/TaN	TaN/Au

Table 7.3: The table shows the three different *on-chip filter* configurations used for measuring the temperature dependency.

7.6 Performance of the build-in filter

As described previously, an *on-chip filter* consisting of two cantilevers inserted in a Wheatstone bridge is used in the chip design. The filter reduces the drift and the noise significantly, but still there is room for improvements. For example, the fact that only the measurement cantilever is coated with gold reduces the efficiency of the filter, since the two cantilevers do not exhibit the same mechanical properties.

In order to optimize the performance of the filter a material with same mechanical properties as gold has to be deposited on the reference cantilever. Moreover, the material has to be inert towards immobilization of molecules containing a thiol-group. No such material was found to be compatible with the fabrication of the chip, and therefore a sandwich of different materials onto both the measurement cantilever and the reference cantilever was proposed, see figure 5.13.

The performance of the improved *on-chip filter* has been tested by measuring the change in surface stress as a function of temperature. The improved *on-chip filter* has been compared to the temperature dependency of an ideal *on-chip filter* with two gold coated cantilevers and an *on-chip filter* with one gold coated cantilever and one non-coated cantilever, see table 7.3.

In figure 7.11 the temperature dependency of the three different *on-chip filter* configurations are shown. The temperature was changed from $T=25\text{ }^{\circ}\text{C}$ to $T=100\text{ }^{\circ}\text{C}$. It is seen from the graph that all three configurations have a very linear temperature dependency. As expected configuration (a) exhibits the highest temperature dependency, but surprisingly the improved *on-chip filter* (c) is less temperature dependent than configuration (b) with the two gold coated cantilevers. The gold-gold configuration the two cantilevers are exactly the same and should in principle not show any temperature dependency. The temperature dependency for configuration (b) on different chips were measured but all tests showed the same temperature dependency. Since the experiments were carried out on version 1 chips, one explanation could be that the gold has been damaged during the processing and thereby exhibits different mechanical properties from cantilever to cantilever. For example the KOH etching might have damaged the gold or there might even be SU-8 residues left on the gold.

Even though configuration (b) showed a higher temperature dependency than expected, it can be concluded from figure 7.11, that the tantalum nitride sandwich structure, con-

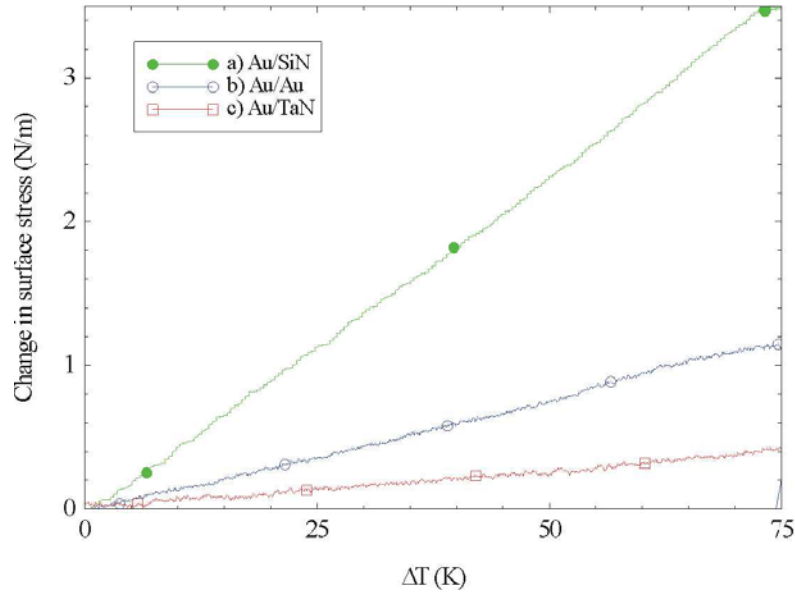


Figure 7.11: The graph shows the temperature dependency of the *on-chip* filter. The temperature dependency has been investigated for different materials on the measurement and the reference cantilever: a) Au-SiN, b) Au-Au and c) Au-TaN. It can be seen that c) has the lowest temperature dependency.

<i>On-chip filter</i>	Temperature sensitivity [10^{-3} N/m·K]
Configuration a	48
Configuration b	16
Configuration c	5

Table 7.4: Temperature sensitivity for three different *on-chip* filter configurations. It can be seen that configuration (c) is about 10 times better than configuration (a).

figuration (c), decreases the temperature dependency of the *on-chip* filter compared to configuration (a). By calculating the slopes from the graphs, the temperature sensitivities can be found. These are given in table 7.4. It can be seen from the table that configuration (c) is about 10 times less temperature sensitive than configuration (a).

It can be concluded from the above experiment that the *on-chip* filter is improved with respect to temperature sensitivity when using the tantalum nitride sandwich layers on the cantilevers. However, more experiments have to be performed in order to determine the over-all performance of the optimized filter.

7.7 Summary

In this chapter the chips were characterized with respect to performance. Optical microscopy was used in order to determine the SU-8 adhesion to the substrate. An adhesion failure of 40 % for the version 1 chips was found. By use of SEM, it was found

that the adhesion failure is due to a design error in the SU-8 mask. The end-point sensitivity and the electrical noise were measured and the actual performance was found to be about 30 % less than expected. The temperature sensitivity of the enhanced *on*-chip filter on the version 2 chips was compared to the temperature sensitivity of the the *on*-chip filter on the version 1 chips. It was found that the improved filter is about 10 times less temperature sensitive.

Chapter 8

Applications

The chip has been tested in various applications in order to test the chip performance. It has not been a goal to perform a detailed investigation of the adsorption kinetics for different molecules, but only to show that the chip works as predicted. First, the measurement setup is presented whereafter the actual noise and drift of the signals are discussed. The chip is tested for its performance when bubbles are introduced in the channel and it is investigated whether it is possible to flow two different samples side by side in the channel. Finally, different experiments are performed by measuring the surface stress change as a function of molecular adsorption or desorption.

8.1 The setup

Before using the chip, it is necessary to place a lid on top of the SU-8 side walls in order to completely close the channel. Since the lid has to be aligned to the chip such that it is possible to wire bond for the electrical connections, a small piece of 80 μm thick lamination film is used as a lid. The lamination film is placed on the SU-8 and by use of a 150 $^{\circ}\text{C}$ hot solder iron the lamination film is welded to the SU-8. This method turned out to be a reproducible method for closing the channel.

The chip is glued into the chip house described in chapter 4 and wire bonding for the electrical connection from the chip to the house is performed. The chip house is placed in a connection box which performs the liquid and electrical connections. A pre-amplifier with an amplification of 1000 and a 100 Hz low pass filter are placed in the box, such that the amplification of the electrical signal is performed very close to the chip. A syringe pump is connected to the box in order to guide the liquid through the channel. The electrical signals from the chip are transferred to a computer. Figure 8.1 shows an optical image of the setup. A program made in LabView is used for the data acquisition. Figure 8.2 shows a photograph of the data acquisition program. The program is capable of acquiring data signals from 5 different Wheatstone bridges simultaneously.

The connection between the chip house and the connection box is not always per-

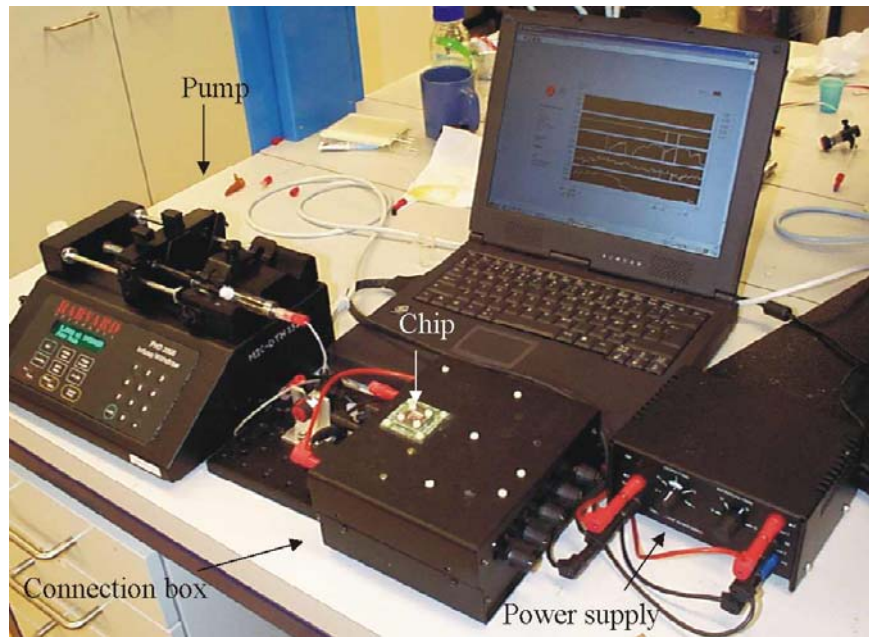


Figure 8.1: Optical image of the measurement setup.

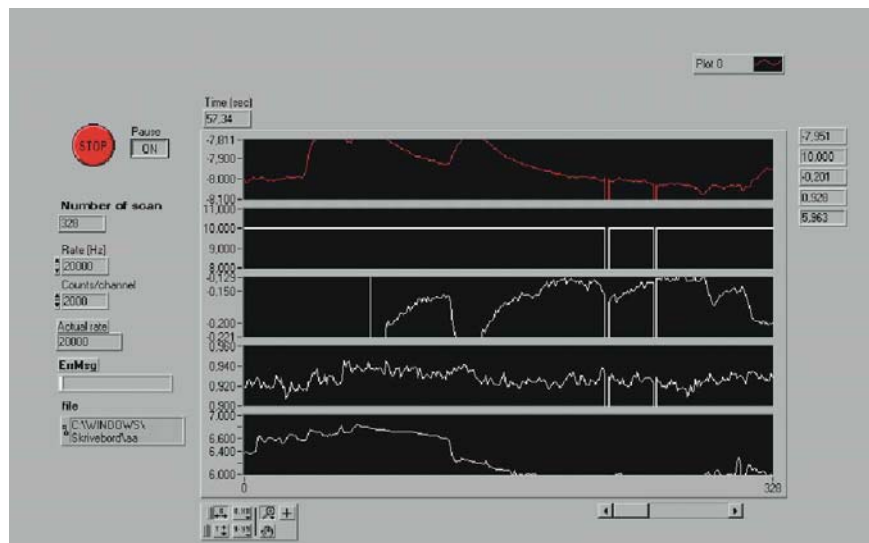


Figure 8.2: Screen-view of the LabView program. 5 signals can be obtained simultaneously. It can be seen that no signal is obtained from number 2 graph from above due to poor electrical connection between chip house and connection box.

fect, which influences the number of Wheatstone bridges from which data is actually acquired. This is due to the fact that the contact between the electrical connection bars on the chip house (see figure 4.9) and the contact pads on the connection box is obtained by a physical contact. If these are mis-aligned no contact is obtained. The average number of Wheatstone bridges that are connected is 3.

8.2 Drift and bubbles

The drift and the noise from the cantilevers are investigated by pumping water with a constant flow rate of $20 \mu\text{L}/\text{min}$ through the channel. After a relaxation time on the order of 5-10 minutes, the drift was reduced to less than the noise floor. The graph in figure 8.3 shows two signals from a version 2 chip. It is seen that the drift is less than the noise floor. The peak-peak noise floor is on the order of $5 \cdot 10^{-2} \text{ N/m}$, which corresponds to about $2 \cdot 10^{-2} \text{ N/m}$ root mean square noise. This is in good correspondence

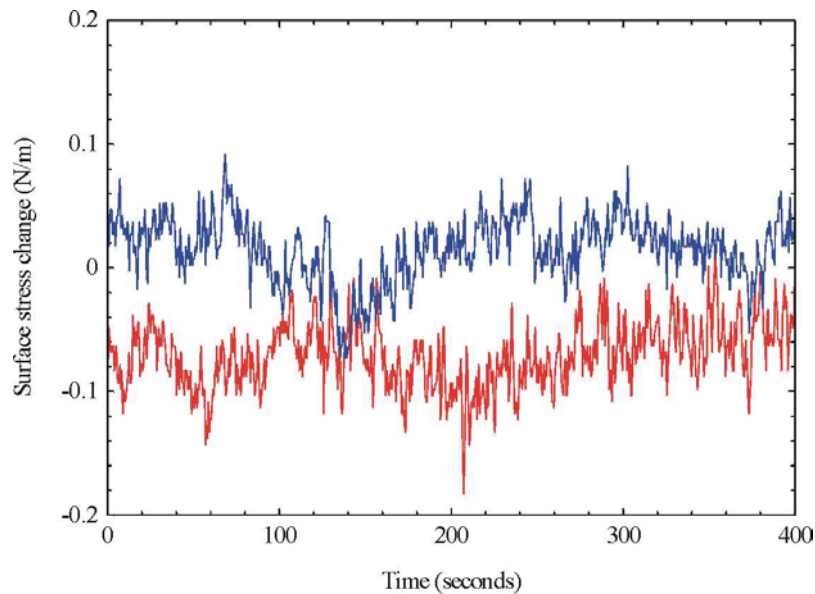


Figure 8.3: *The graph shows signals from two Wheatstone bridges. It is seen that the drift is comparable to the noise floor.*

with the noise floor measured previously in chapter 7.

A critical phenomenon often observed in micro liquid handling systems is bubbles. These might destroy the measurements or even the micro channels, due to the high surface tension of water. If bubbles are introduced into a micro channel the bubbles will stay at places with the lowest flow resistance. For example, the flow resistance is increased at the channel junction from the $400 \mu\text{m}$ wide channel to the $200 \mu\text{m}$ wide channel in this chip design, and bubbles therefore tend to stay at the channel junction. In order to get rid of the bubbles the flow rate has to be increased significantly.

An experiment is performed in order to investigate what happens to the cantilever when a bubble flows through the channel. A worst case scenario is that the cantilevers break. This will make the chip very sensitive to the setup, since bubbles might be introduced when shifting between liquids. Figure 8.4 shows a series of optical images of a bubble passing by the cantilevers in the channel. The arrow indicates the front of the bubble. It is observed that the cantilevers do not break when bubbles travel

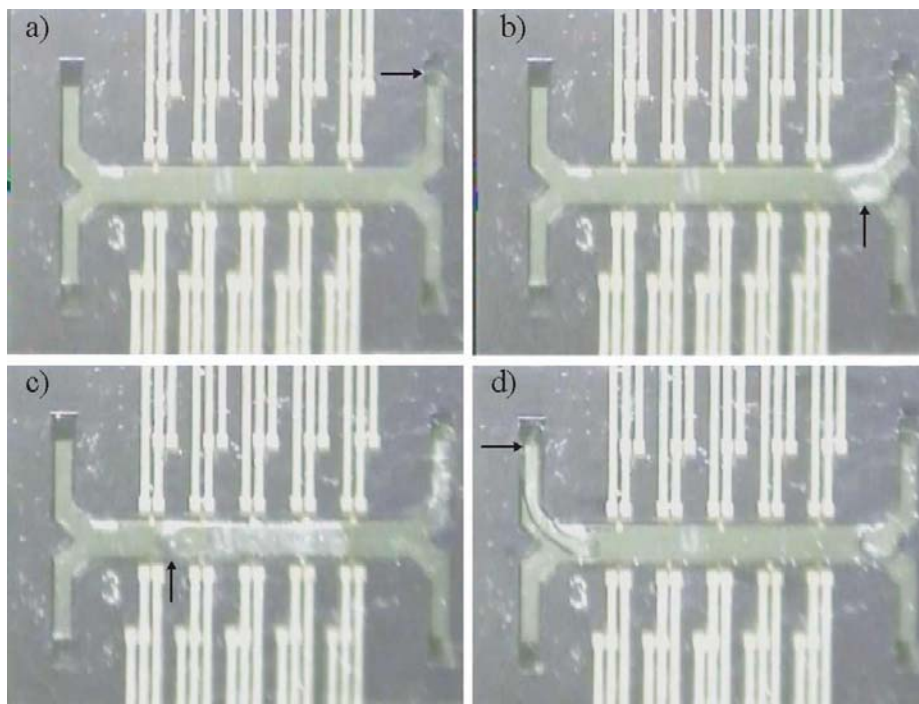


Figure 8.4: The figure shows a series of optical images of a bubble passing by the cantilevers. The arrow indicates the front of the bubble.

through the channel. Even for very high flow rates, and thereby high bubble speed nothing happens to the cantilevers except for a very large signal due to a bending when the bubbles pass by, see figure 8.6.

8.2.1 Two liquids in the channel

As described in chapter 4 the chip is designed with two inlets and two outlets. The reason for this design is to be able to flow two different liquids side by side in the channel simultaneously. This can for example be used for immobilization of two different types of molecules on the cantilevers or to measure the difference in molecule concentration in a test and a reference sample. Since the flow is in the laminar flow regime, mixing is only obtained due to diffusion which is normally slower than the time it takes the liquid to move through the channel.

An experiment for the investigation of whether it is possible to flow two different liquids through the channel is performed. In figure 8.5 an optical image of the channel is seen. The color difference in the channel is due to two liquids with different colors running in the channel. The flow rate in the experiment is set to $20 \mu\text{L}/\text{min}$. The flow rate at which the liquid was found to mix due to diffusion was found to be less than $1 \mu\text{L}/\text{min}$.

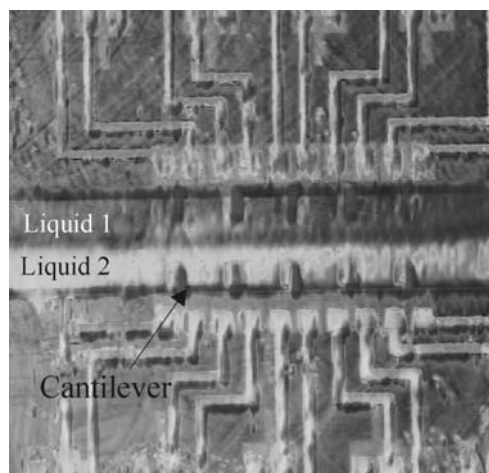


Figure 8.5: *Optical image of two liquids with different colors in the channel.*

8.3 Determination of build-in stress in metal films

The metal layers on the measurement cantilever have been etched away as an experiment in order to determine the build-in stress in the metal films. Moreover, it is possible to investigate the performance of the chip during the experiments with respect to reproducibility and sensitivity.

8.3.1 Build-in stress in a gold film

A chip from version 1 was used in order to investigate the build-in stress in the gold layer on the measurement cantilever. After purging the chip with water in order to stabilize the signal, a 1:3, aqua regia:water solution is introduced into the channel for 60 seconds. This solution selectively etches the gold film on the measurement cantilever. Figure 8.6 shows the resulting graph from the experiment.

The aqua regia solution is introduced immediately after a bubble. The effect on the signal due to the bubble is seen to be a very large amplitude deflection. It is seen from the graph that the surface stress change on the measurement cantilevers begins immediately after the bubble. The Wheatstone bridges have been set up into two configurations, see figure 8.7. As seen from the figure the difference in the two configurations is that the supply voltage has been reversed. The reason for this is to make sure that the signals in fact reflect an etching of the gold instead of just a drift in the system. When molecules are adsorbed on the surface of the measurement cantilever, a negative signal is obtained for configuration A if the surface stress is tensile.

The signals from the 4 curves follow each other closely. The reason for the variation in the amplitude is probably due to the fact that the gold film has not been completely clean before performing the experiment. As will be seen later, this turns out to be a problem when immobilizing other types of molecules.

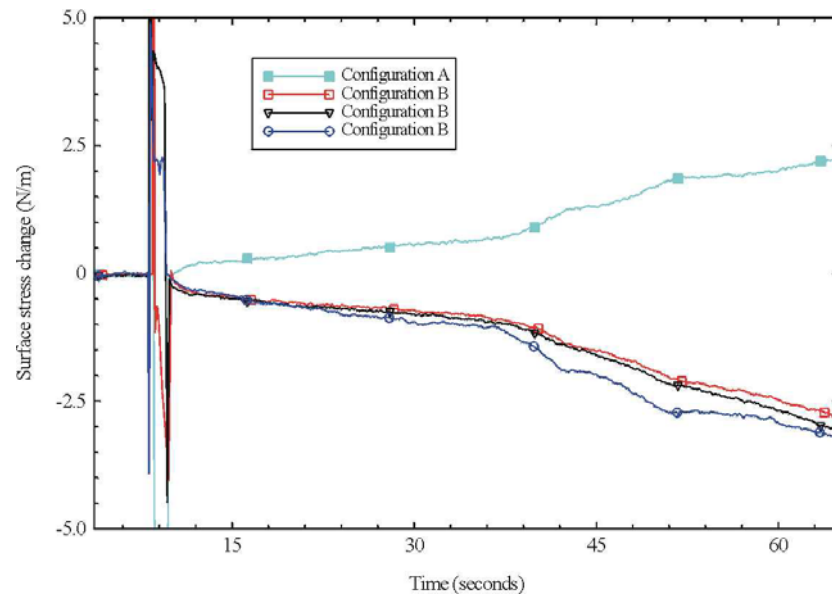


Figure 8.6: The graph shows four Wheatstone bridge signals when an aqua regia solution is introduced into the channel.

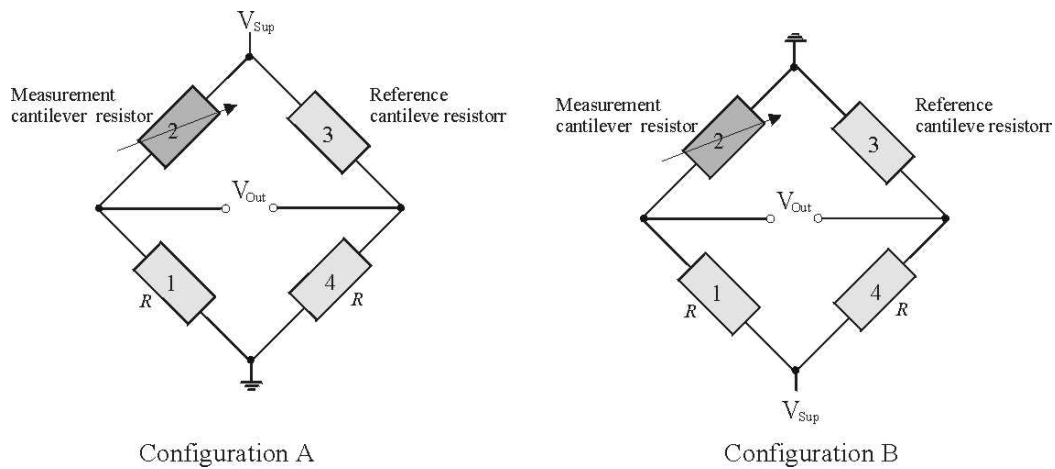


Figure 8.7: The figure shows the two Wheatstone bridge configurations used in the measurements. The difference is that the supply voltage has been reversed.

From the graph, it is possible to determine the build-in stress in the gold layer. The gold layer has an initial thickness of 40 nm. About 20 nm of the gold was etched away during the experiment since the aqua regia was only in contact with the cantilevers for 60 seconds. The maximum change in surface stress can be measured to about 2.7 N/m. Since the signal is negative for configuration B, the build-in stress can be calculated to 135 MPa tensile stress.

The stress level in the gold film can be calculated by assuming that the stress is due to the fact that gold has a higher thermal expansion coefficient κ_{Au} than the cantilever materials. During the version 1 chip fabrication, the gold on the cantilevers are exposed to a temperature of about $T = 150$ °C. Assuming that the gold film is stress released at this temperature the build-in stress in the gold at room temperature can be calculated from the following expression:

$$\sigma_{Au} = \Delta\kappa_{Au,SiN} \cdot \Delta T \cdot E_{Au} \quad (8.3-1)$$

It is assumed that the thermal expansion coefficient for the cantilever equals the thermal expansion coefficient for silicon nitride, κ_{SiN} . Since $\kappa_{SiN} = 2.5 \cdot 10^{-6}$, $\kappa_{Au} = 14.5 \cdot 10^{-6}$, $\Delta T = 150$ °C - 20 °C = 130 °C and $E_{Au} = 79$ MPa, the build-in stress can be calculated to $\sigma_{Au} = 123$ MPa. The difference between the calculated and measured build-in stress in the gold film is about 10 %. The difference might be due to the temperature dependency of the thermal expansion coefficient and on the expected gold film thickness after the etching.

8.3.2 Build-in stress in a nickel film

In this section the build-in stress in a nickel film is investigated by the same method as used above. A chip from version 2 in which all the cantilevers are nickel coated is used. The nickel is supposed to be removed from the cantilevers immediately before a measurement is performed in order to protect the gold. A nickel etch test on a clean wafer with a nickel pattern is performed by using an etch solution consisting of 20ml:80ml HCl:H₂O + 3 g CuSO₄. The 30 nm nickel film is etched away after 30 seconds. The nickel on the chip was not that easy to remove. This is probably because a nickel oxide has been formed on the nickel during the 250 °C annealing before the SU-8 deposition. Also some SU-8 residues might have been left on the nickel surface which makes it even more difficult to remove the nickel from the cantilevers.

During the nickel etching it is observed that the nickel on the reference cantilever and thereby on the tantalum nitride is easier to remove than on the gold coated measurement cantilevers. The reason for this is not understood completely, but it makes it possible to measure the change in surface stress during the nickel etch on either the measurement cantilevers or on the reference cantilevers. In figure 8.8 the surface stress change is measured as a function of the nickel etching on the measurement cantilevers. The etching solution is introduced at about $t=100$ seconds. The Wheatstone bridge configurations A and B are equal to the ones illustrated in figure 8.7, while Wheatstone bridge configuration C equals configuration A except that the measurement cantilever is substituted with another reference cantilever. No signal is supposed to be observed from this configuration which is in agreement with the graph.

From the curves of configuration A and B the stress in the 30 nm thick nickel film is calculated to approximately 1000 MPa tensile stress by the maximum surface stress value from the graph.

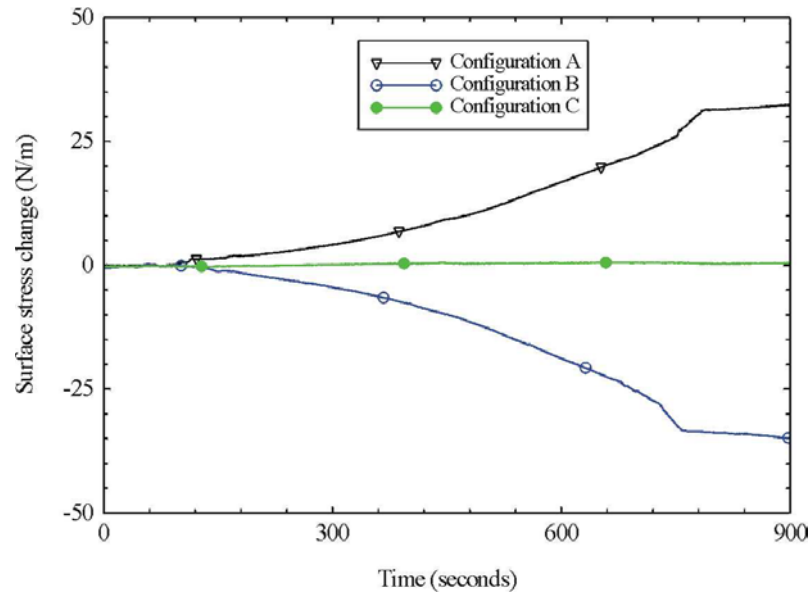


Figure 8.8: The figure shows the change in surface stress as a function of nickel etching on the measurement cantilever.

This result can be compared with the expected build-in stress by the same method as used for determining the build-in stress in the gold film. Assuming that the nickel film is stress released at $T = 250\text{ }^{\circ}\text{C}$, which the nickel is exposed to during the fabrication of the version 2 chips, the build-in stress in the nickel film at room temperature can be calculated by use of equation 8.3-1 to $\sigma_{Ni} = 845\text{ MPa}$, when $\kappa_{Ni} = 17.2 \cdot 10^{-6}$, $\Delta T = 250\text{ }^{\circ}\text{C} - 20\text{ }^{\circ}\text{C} = 230\text{ }^{\circ}\text{C}$ and $E_{Ni} = 250\text{ MPa}$. The difference between the calculated and the measured build-in stress value is about 15 %. This difference is probably also due to the temperature dependency of the thermal expansion coefficient.

The results from the measurements of the build-in stresses in the gold and nickel film, are both in good agreement with the calculated values. It can therefore be concluded that the model for the surface stress sensitive cantilever developed in chapter 2 is in good agreement with the actual behavior of the cantilever when exposed to a surface stress change.

8.4 Immobilization by sulphur binding

Using sulphur atoms for the binding of proteins and DNA molecules to gold is a well known and extensively used technique in biotechnology. Molecules modified to carry a sulphur atom, or more precisely a thiol group (-SH) are commercial available, as in for example thiol-modified oligos.

The sulphur binding to gold is very specific. This specificity makes it possible to confine for example thiol-modified oligos on only one cantilever, by designing the cantilevers

such that only the measurement cantilever is gold coated on one side.

Molecules carrying thiol groups are known to adsorb on gold and assemble in a monolayer in order to optimize the packing on the surface. The immobilization of thiol-modified molecules is to some extent a self-terminating process and the density of molecules on the surface is relatively easy to control and reproduce.

For the above mentioned reasons, thiol-modified or thiol containing molecules are used in this thesis to demonstrate the chips possibility to measure the immobilization of molecules onto the measurement cantilever.

8.5 Immobilization experiments

In this section three different molecule immobilization experiments are discussed. Chips from both version 1 and version 2 are used in the experiments. During experiments with chips from version 1 it was observed that the immobilization on the gold film on the measurement cantilever is difficult to perform. The gold surface is probably contaminated due to fact that is not protected during the fabrication steps. It has also been observed that gold exposed to atmospheric air is contaminated which reduces the immobilization of the thiol-modified molecules. The contamination on the gold film on the measurement cantilevers in the version 1 chips was removed by etching a part of the gold in a mild aqua regia solution (1:3 Aqua regia:water) immediately before using the chip. Unfortunately, this cleaning method is not reliable since the etch rate of the aqua regia is highly dependent on the amount of contaminations. As described previously, the fabrication of version 2 chips was changed such that the gold is protected by a thin nickel layer which is etched away selectively to the gold immediately before using the cantilevers leaving a clean gold surface.

8.5.1 Immobilization of octadecanethiol

The octadecanethiol, $CH_3(CH_2)_{17}SH$ is known to form a stable, dense and highly structured monolayer on gold [104] due to the sulphur gold interaction.

After etching away the nickel on a version 2 chip, a buffer consisting of 2:1 H_2O :ethanol is pumped through the channel with a speed of $20 \mu L/min$. A stabilized flow is obtained after about 10 minutes and a $1 \mu M$ octadecanethiol concentration in the 2:1 H_2O :ethanol buffer is then introduced into the channel. The change in surface stress as a function of time is shown in the graph in figure 8.9. The graph shows the signals from three Wheatstone bridge configurations. The octadecanethiol solution is introduced at $t=20$ seconds and the signal is stabilized at about $t=100$ seconds. The surface stress change is on the order of $0.5 N/m$ tensile stress. This result is in good agreement with the work performed by A. Hansen in [105].

From this experiment it can be concluded that the gold coated cantilevers are sensitive

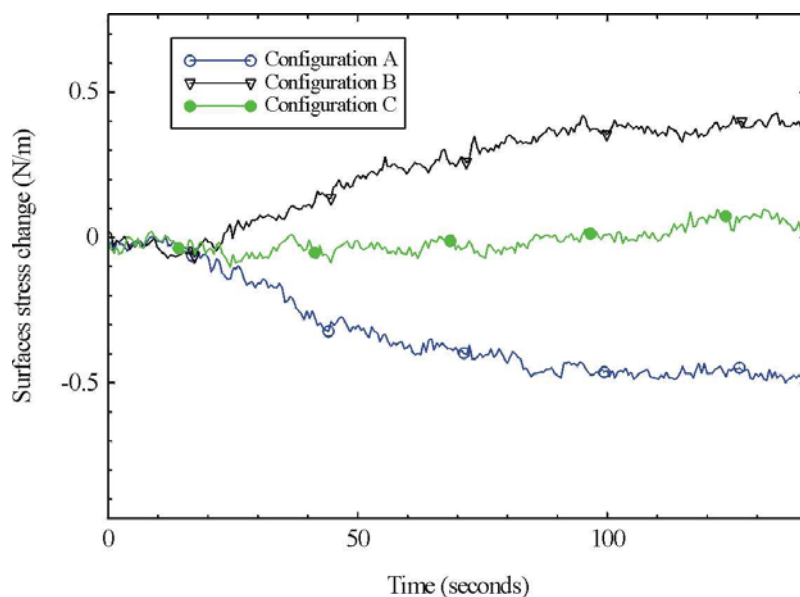


Figure 8.9: The graph shows the signals obtained from the three Wheatstone bridge configuration when a $1\ \mu\text{M}$ octadecanethiol solution is pumped through the channel.

to surface stress changes when a monolayer of a simple molecule is immobilized on the surface.

8.5.2 Immobilization of cysteine

An antibody is a protein that binds to an antigen with high specificity. A well-known example is that the humane body develops its own antibodies against disease related antigens. When the antibodies bind to the disease related antigen it makes it ineffective and a potential disease is suppressed.

By immobilizing antibodies onto the measurement cantilever surface it is in principle possible to detect the antibody-antigen reaction. However, when antibodies are immobilized on a solid-phase surface, their binding activity is usually less than that of soluble antibodies. A reason for this is probably due to the random orientation of the antibody molecule on the solid-phase surface. It is therefore necessary to develop methods for orientation dependent immobilization of the antibody.

It is well-known that protein engineering makes it possible to introduce a small molecule called cysteine into the protein site specifically [106, 107]. Cysteine includes a sulfur molecule and thereby the self-assembly thiol-gold phenomenon is obtained.

It is out of the scope of this thesis to investigate an antigen-antibody reaction using the cantilever chip, but instead an experiment of immobilizing cysteine onto the gold coated measurement cantilever surface is performed in order to show the potential of

immobilizing for example antibody on the cantilever.

The nickel is etched away from the cantilevers on a version 2 chip. Hereafter a buffer consisting of 10 mM KH_2PO_4 is pumped through the channel until the signals from the Wheatstone bridges have stabilized. A 0.7 mM cysteine concentration in the buffer is pumped through the channel at a flow rate of $20 \mu L/min$. The result is shown in figure 8.10. The graph shows the Wheatstone signals from configuration A and B. Un-

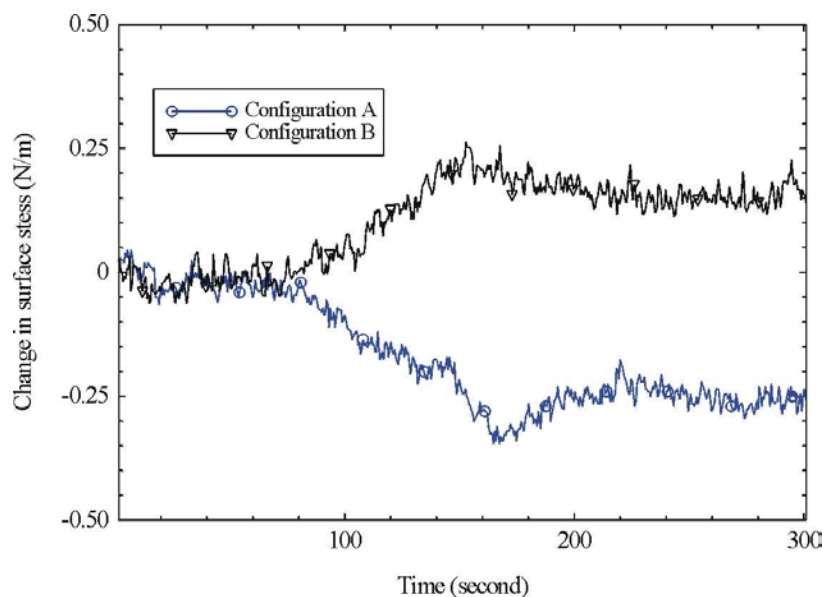


Figure 8.10: The graph shows the signals obtained from Wheatstone bridge configuration A and B when a 0.7 mM cysteine solution is pumped through the channel.

fortunately, a signal from Wheatstone bridge configuration C was not obtained. The cysteine solution is introduced at $t=75$ seconds, and the signal is stabilized after about $t=220$ seconds. The signal peaks at a tensile surface stress change of 0.35 N/m, whereafter it is reduced to 0.25 N/m. The reason for this is not completely understood, but other experiments indicates that the peak at the 0.35 N/m corresponds to the surface stress change due to cysteine immobilization. The reason for the decay is probably due to a drift in the signal. The result is in good agreement with the work performed by A. Hansen [105].

The experiment shows that it is possible to obtain a signal when immobilizing cysteine molecules which includes sulphur molecules. The experiment shows the chip's potential for on-line monitoring of for example antibody immobilization.

8.5.3 Thiol-oligo immobilization

Diagnostic of genetic related diseases is a very hot topic both within research and in the media. Normally, a genetic analysis requires a lot of pre-treatment before the detection

is performed. The method is both expensive due to the necessary equipment and time consuming. A reduction of the product cost as well as the portability of the analytical equipment would make it possible to perform the analysis in the doctors office. This is especially interesting for genetic diseases where an early diagnose enables efficient treatment. Such systems have a high advantage compared to the common diagnostic methods.

Since the cantilever-based biochemical sensor has the potential as a cheap *point-of-care* apparatus, an experiment measuring the immobilization of thiol modified DNA-oligos is performed. In the experiment 25'mers long thiol-modified oligos are used. The oligos are commercially available and a detailed description of the oligos is presented in [56].

A version 1 chip is used in this experiment, since a version 2 chip was not finished when this experiment was performed. The gold on the measurement cantilever is cleaned in an aqua regia solution whereafter DI water is pumped through the system until the signal is stabilized. A $10\text{ }\mu\text{M}$ oligo solution is then pumped through the channel with a flow rate of $20\text{ }\mu\text{L}/\text{min}$ and the signal from the Wheatstone bridges are picked up by the computer.

Figure 8.11 shows the resulting graph. The signals from two Wheatstone bridge configuration A are seen in the graph. The oligo solution is introduced at $t=0$ seconds. The signals stabilize at about $t=80$ seconds where the compressive change in surface

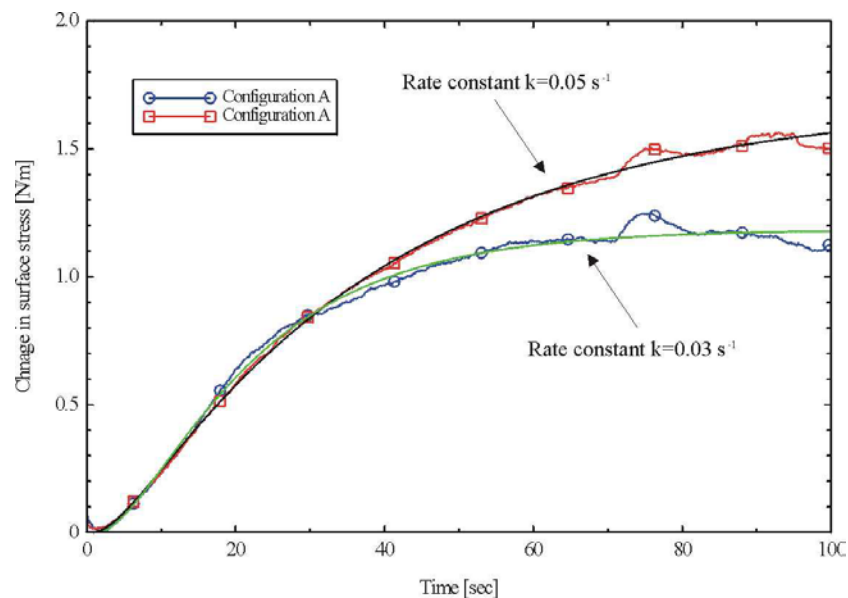


Figure 8.11: The graph shows the signals obtained from the two Wheatstone bridge configurations when a $10\text{ }\mu\text{M}$ oligo solution is pumped through the channel.

stress has reach a level of about 1.3 N/m . The two signals do not reach exactly the

same level. Probably, the aqua regia cleaning method leaves a quite rough gold surface due to the contaminants, which corresponds to the results obtained by A. Hansen *et al.* [54]. The effective gold surface is therefore dependent on the amount of contaminants before the cleaning. The more rough the surface is, the larger effective surface is obtained. By using the nickel protection layer, this effect is probably suppressed.

Previous work on measuring the adsorption of thiol-modified oligos on gold has been reported by R. Marie *et al.* [56]. In this case the adsorption curves are fitted with an isotherm adsorption model. In this model the molecules are in excess in the solution compared to the number of molecules necessary to cover the surface. The surface stress change of the cantilever can then be modeled by a sum of two so-called Langmuir functions

$$y = a_1(1 - \exp(-k_1 \cdot t)) + a_2(1 - \exp(-k_2 \cdot t)) \quad (8.5-1)$$

where a_1 and a_2 are the signal amplitude constants, while k_1 and k_2 are the rate constants. This model has also been used to describe the adsorption of alkanethiols on gold using cantilever sensor [39]. Both functions in expression 8.5-1 obey the model of a single isotherm. The first isotherm describes the desorption of the contaminants on the cantilever. The reason why the contaminants are desorbed is because of the thiol molecules stronger binding energy. The second isotherm describes the adsorption of the thiol-modified oligos. The two isotherms corresponds to different kinetics. Since the desorption has a higher rate constant k_1 than the adsorption k_2 the curve has a minimum before stabilizing. In figure 8.11 the minimum is obtained at $t = 5$ s. The graphs have been fitted to the model in equation 8.5-1 and the adsorption coefficient has been found to $k = 0.03$ s⁻¹ and $k = 0.05$ s⁻¹, see figure 8.11. This result is in very good agreement with the work performed by R. Marie in [56], where the rate constant is measured to $k = 0.05$ s⁻¹.

The experiment shows that it is possible to measure the surface stress change when 25'mers thiol-modified oligos are immobilized on the measurement cantilever. The detection of DNA hybridization has not been performed using the cantilever chip. Other work [43, 108, 42] shows that it is possible to detect surface stress changes also when the hybridization is performed.

8.6 Summary

In this chapter some experiments performed using the cantilever-based biochemical sensor integrated in a micro liquid handling system are discussed. The cantilever signals were found to stabilize after about 10 minutes and the measured electrical noise corresponds to the noise level found in chapter 7. The cantilevers do not break when exposed to bubbles in the channel. By etching the gold and nickel away from the measurement cantilevers, the build-in stress in these layers was determined, and finally the chip was used to measure the change in surface stress due to the adsorption of thiol-modified bio-chemical molecules, including cysteine, octadecanethiol and thiol-modified DNA-oligos.

Chapter 9

Conclusions

The three major goals of this thesis have been: To develop a new theory that describes the behavior of a cantilever-based biochemical sensor with piezoresistive readout; to design and fabricate the first cantilever-based biochemical sensor integrated into a micro liquid handling system and to prove the working principle of the chip. All the three subjects have been discussed and successfully fulfilled in this project.

From the theory describing the surface stress sensitive cantilever with piezoresistive readout it was found that the cantilever and resistor length and width do not have any influence on the sensitivity. The only important parameters were found to be the cantilever thickness, the stiffness and the position of the resistor with respect to the neutral axis. This result is different from the theory describing the end-point deflection sensitive cantilever used in for example AFM, where the sensitivity is also highly dependent on the cantilever length. Since the strain is not symmetrical around the neutral axis when the cantilever is exposed to a surface stress, the resistor has to be placed on the same side of the neutral axis as the acting surface stress in order to obtain the highest sensitivity.

In order to optimize the performance of the surface stress sensitive cantilever, an investigation of the gauge factor and the $1/f$ noise in single crystalline silicon and poly crystalline silicon with different grain sizes has been performed. For the best performance, it is important to optimize the signal to noise ratio rather than the sensitivity. Even though low doped single crystalline silicon exhibits a larger gauge factor than highly doped single crystalline silicon, it was found that highly doped single crystalline silicon exhibits almost a factor of 2 higher signal to noise ratio than low doped single crystalline silicon. The same trend was observed for poly crystalline silicon. Here it was found that highly doped microcrystalline silicon exhibits an almost a factor of 2 larger signal to noise ratio than low doped amorphous silicon. The difference in the signal to noise ratio between a poly crystalline silicon resistor and a single crystalline silicon resistor was found to be a factor of 10.

The design of the cantilever was optimized, and a minimum detectable surface stress change was calculated to $5.7 \cdot 10^{-5}$ N/m for a cantilever with a single crystalline silicon

piezoresistor, while the minimum detectable surface stress change for a cantilever with a poly crystalline silicon resistor was calculated to $2.6 \cdot 10^{-4}$ N/m.

The cantilever-based biochemical sensor integrated in a micro liquid handling system has been designed to include 10 cantilevers in a 3 mm long channel. Half of the cantilevers are coated with a gold layer in order to functionalize them for immobilization of molecules which contain sulphur atoms. The other half of the cantilevers are used as reference cantilevers in an *on*-chip filter. The chip is designed in a way such that only laminar flow is allowed in the channel at reasonable flow rates. Five different chip designs have been included in the mask lay-out.

It was decided to use poly crystalline silicon as resistor material in the fabrication of the cantilevers in this thesis. Poly crystalline silicon resistors are easier to realize than single crystalline silicon resistors, which would require the use of SOI wafers. The chips with poly silicon resistors can be seen as a proof of the detector principle. If desired the signal to noise ration can later be improved by using single crystalline silicon resistors.

Two versions of the chips were successfully fabricated in this project. To the author's knowledge, this is the first time such a sensor has been fabricated. During the fabrication of the first version some minor design errors were discovered and changes were successfully implemented in the second fabrication version. The second version of the chips, also includes an optimized reference cantilever which improves the *on*-chip filter by a factor of 10.

In order to investigate whether this new sensor type performs as expected, it has been characterized with respect to signal to noise ratio and it was seen that the chips with design 1 cantilevers have a minimum detectable surface stress change of $1.8 \cdot 10^{-2}$ N/m. Initial experiments monitoring surface stress changes due to metal removal and molecular adsorption have furthermore been performed. The metal films on the measurement cantilever were etched away and the resulting changes in surface stress were measured simultaneously. From the theory developed for the surface stress sensitive cantilever, the build-in stresses in the metal films were calculated. The results correspond very well with the theoretically expected stress values. Since the objective of the sensor is to monitor the change in surface stress when molecules are immobilized onto the sensor surface, preliminary experiments of immobilization of three different molecules: octadecanethiol, cystein and DNA-oligis were performed.

During this thesis, a detailed knowledge was obtained on the processing of the cantilever-based biochemical sensor integrated in a micro liquid handling system. It is strongly believed that the fabrication can be optimized further such that the chip can be fabricated with a very high yield. The sensor described in this thesis is not optimized completely with respect to minimum detectable surface stress, and therefore does not exhibit the highest resolution that can be obtained with a piezoresistive cantilever. It is believed that an optimized sensor can be designed fairly easy with the knowledge obtained in this thesis.

The potential of the cantilever-based biochemical sensor with piezoresistive readout is large. Due to its size, the fast response time, the sensitivity and the simple readout mechanism from even large arrays of cantilevers, the sensor is for example suitable for *point of care* in-vitro diagnostics. Furthermore, the fact that the surface stress change can be monitored on-line, the sensor is a strong research tool for the investigation of molecules surface kinetic during immobilization onto the cantilever surface. The perspective of the cantilever-based biochemical sensor is large, and it is believed that the on-going research and development with-in this field will result in many new applications. Eventually, the cantilever-based biochemical sensor will probably also be commercialized.

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Appendix A

List of publications

In the course of this Ph.D. project the following conference and journal papers have been published.

- J. Thaysen, A. Boisen, O. Hansen and S. Bouwstra. Atomic force microscopy probe with piezoresistive read-out and a highly symmetrical Wheatstone bridge arrangement. *International Conference on Solid-State Sensors and Actuators, Proceedings*, 2:1852-1855, 1999.
- J. Thaysen, A. Boisen, O. Hansen and S. Bouwstra. Atomic force microscopy probe with piezoresistive read-out and a highly symmetrical Wheatstone bridge arrangement. *Sensors and Actuators A: Physical*, 83: 47-53, 2000.
- A. Boisen, J. Thaysen, H. Jensenius and O. Hansen. Environmental sensors based on micromachined cantilevers with piezoresistive read-out. *Ultramicroscopy*, 82(1-4):1-9, 2000.
- H. Jensenius, J. Thaysen, A.A. Rasmussen, L.H. Veje, O. Hansen and A. Boisen. A microcantilever-based alcohol vapor sensor-application and response model. *Applied Physics Letters*, 76(18):2615-17, 2000.
- H. Jensenius, J. Thaysen, A.A. Rasmussen, L.H. Veje, O. Hansen and A. Boisen. Gas sensor based on micromachined cantilevers with integrated read-out. *Conference on Scanning Tunneling Microscopy/Spectroscopy and Related Proximal Probe Microscopy, (STM'99), Proceedings*, 586-587, 1999.
- P.A. Rasmussen, J. Thaysen, S. Bouwstra and A. Boisen, Piezoresistive atomic force microscopy probe with sputtered silicon tip. *The 14th European Conference on Solid-State Transducers, Proceedings*, 637-640, 2000.
- P.A. Rasmussen, J. Thaysen, S. Bouwstra and A. Boisen, Modular design of AFM probe with sputtered silicon tip. *Sensors and Actuators A: Physical*, 2959:1-6, 2001
- J. Thaysen, R. Marie and A. Boisen. Cantilever-based bio-chemical sensor integrated in a microliquid handling system. *The 14th IEEE International Conference on Micro Electro Mechanical Systems, Proceedings*, 401-404, 2001.

- J. Thaysen and A. Boisen. A microcantilever-based detection principle for mTAS. *Accepted for the Fifth International Conference on Miniaturized Chemical and Biochemical Analysis Systems 2001.*

Appendix B

Process sequence (version 2)

Wafers: 7 wafer (OP51) 350 μm double sided polished.

1. **Deposition of nitride:** BHF dip for 30 sec. LPCVD low stress nitride: 93 sccm SiH_2Cl_2 , 13 sccm NH_3 , 13 min at 835 $^\circ\text{C}$, yields a nitride thickness of about 550 \AA . Thickness measured by ellipsiometer: 550 \AA .
2. **Polysilicon:** Process recipe: Poly, 80 sccm Silane, $p = 250$ mTorr, $T = 580$ $^\circ\text{C}$. Deposition time: 33 min, deposition rate ~ 90 $\text{\AA}/\text{min}$, which yields a polysilicon thickness of 1500 \AA .
3. **Resist:** HMDS furnace in 30 min. 1.5 μm resist is spun on the front side of the wafers. Postbaked in oven at 120 $^\circ\text{C}$ for 25 min.
4. **Poly-Si etch:** The backside silicon is removed in a 1:1:0.05 $\text{H}_2\text{O}:\text{HN}_3:\text{BHF}$ solution for 3 min.
5. **Strip of resist:** The resist is stripped in acetone for 2 min + 30 min Ashing (1000 W + 210 sccm O_2).
6. **Boron implantation:** The wafers is boron ion implanted by the settings: Boron dose: $5 \cdot 10^{14} \text{ cm}^{-2}$, implantation energy: 30 keV.
7. **Resist:** HMDS furnace in 30 min. 1.5 μm resist is spun on the front side of the wafers.
8. **Photolithography:** Mask 1 (Resistor) is placed in the aligner. Aligner settings: Hard contact, Expose with UV light for 10 sec. The wafers is developed in a 1 AZ 351B : 5 DI water solution for 60 seconds at 22 $^\circ\text{C}$.
9. **RIE etch of polysilicon:** The poly crystalline silicon is etched in order to define the resistors. Recipe: AB-ISO, 40 sccm SF_6 , $p = 80$ mTorr, $P = 30$ W, in 50 sec. The etched time is controlled by an end-point signal.
10. **Strip of resist:** The resist is stripped in acetone for 2 min.

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11. **Resist:** HMDS oven for 30 min. Hoechst AZ 5214E resist is spun on the front side of the wafers at 4500 rpm for 20 sec, whereafter the wafers is prebaked for 1 min at 90 °C. The resist thickness becomes 1.5 μm .
 12. **Photolithography:** Mask 2 (Implantation) is placed in the aligner. Aligner settings: prox, Expose with UV light for 10 sec. The wafers is developed in a 1 AZ 351B : 5 DI water solution for 60 seconds at 22 °C.
 13. **Hard baking:** The resist is hardbaked in an 120 C oven for 25 min.
 14. **Boron implantation:** The wafers is boron ion implanted by the settings: Boron dose: $5 \cdot 10^{15} \text{ cm}^{-2}$, implantation energy: 30 keV
 15. **Strip of resist:** The resist is stripped in the asher for 30 min.
 16. **Deposition of nitride:** RCA clean + 10 dummy, LPCVD low stress nitride: 93 sccm SiH_2Cl_2 , 13 sccm NH_3 , 66 min at 835 °C, yields a nitride thickness of about 2800 Å. The depo. time is 64 min, yielding a dep. rate at 43.5 Å/min Thickness measured by ellipsiometer: 2810 Å.
 17. **Resist:** HMDS furnace in 30 min. 1.5 μm resist is spun on the **backside** of the wafers.
 18. **Photolithography:** Mask 3 (Backside) is placed in the aligner. Aligner settings: backsidealignment, hardcontact, Expose with UV light for 10 sec. The wafers is developed in a 1 AZ 351B : 5 DI water solution for 60 seconds at 22 °C.
 19. **RIE of nitride:** The RIE chamber is cleaned by use of the recipe PR_STRIP for 10 min. The wafers are etched by an anisotropy silicon etch JT_NITR3, with the settings: 43 sccm N_2 , 8 sccm CHF_3 , $p = 38 \text{ mTorr}$ and $P = 60 \text{ W}$. Etch time: 10 min, etch rate: 380 Å/min selectivity 1.7.
 20. **Strip of resist:** The resist is stripped in acetone for 2 min.
 21. **KOH etch:** The backside is now etched in KOH at 80 C, so a 90 μm membrane is remaining: etch rate: 1,3 $\mu\text{m}/\text{min}$, etch time: 200 min.
 22. **Photolithography:** Mask 4 (Channel) is placed in the aligner. Aligner settings: hardcontact, Expose with UV light for 10 sec. The wafers is developed in a 1 AZ 351B : 5 DI water solution for 60 seconds at 22 °C.
 23. **RIE of nitride:** The RIE chamber is cleaned by use of the recipe PR_STRIP for 10 min. The wafers are etched by an anisotropy silicon etch JT_NITR3, with the settings: 43 sccm N_2 , 8 sccm CHF_3 , $p = 38 \text{ mTorr}$ and $P = 60 \text{ W}$. Etch time: 8.15 min, etch rate: 430 Å/min selectivity 1.7.
 24. **Strip of resist:** The resist is stripped in acetone for 2 min.

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25. **Deposition of TEOS:** RCA clean, TEOS: 50 sccm, O₂:30 sccm, p=190 mTorr, T=725 °C. depo. time: 65 min yields a thickness of about 7000 Å. Thickness measured by ellipsiometer: 7160 Å
 26. **Resist:** HMDS furnace in 30 min. 1.5 μm resist is spun on the frontside of the wafers.
 27. **Photolithography:** Mask 5 (TEOS) is placed in the aligner. Aligner settings: hardcontact, Expose with UV light for 10 sec. The wafers is developed in a 1 AZ 351B : 5 DI water solution for 60 seconds at 22 °C.
 28. **Hardbaking:** The resist is hardbaked at 120 C in 25 min
 29. **Etch of TEOS:** The TEOS is etch in BHF for 10 min
 30. **Strip of resist:** The resist is stripped in the asher
 31. **Resist:** HMDS furnace in 30 min. 1.5 μm resist is spun on the frontside of the wafers.
 32. **Photolithography:** Mask 5 (Imm. metal) is placed in the aligner. Aligner settings: hardcontact, Expose with UV light for 10 sec. The wafers is developed in a 1 AZ 351B : 5 DI water solution for 60 seconds at 22 °C.
 33. **Sputtering of TaN:** 150 Å TaN is co-sputtered from a tantalum target. Ar: 15 sccm, N₂: 15 sccm, p=0.4 Pa. Deposition rate: 17 Å/min.
 34. **Evaporation of metal:** The wafer is first clean in a argon plasma at P=100 W in 5 minutes whereafter 20 Å Cr + 400 Å Au + 300 Å nickel is evaporated on the wafer without breaking the vacuum.
 35. **Lift-off:** The metal is lifted in a ultrasonic acetone holder
 36. **Resist:** HMDS furnace in 30 min. 1.5 μm resist is spun on the frontside of the wafers.
 37. **Photolithography:** Mask 6 (dummy. metal) is placed in the aligner. Aligner settings: hardcontact, Expose with UV light for 10 sec. The wafers is developed in a 1 AZ 351B : 5 DI water solution for 60 seconds at 22 °C.
 38. **Evaporation of metal:** 20 Å Cr + 400 Å Au is evaporated on the wafer without breaking the vacuum.
 39. **Sputtering of TaN:** 150 Å TaN is co-sputtered from a tantalum target. Ar: 15 sccm, N₂: 15 sccm, p=0.4 Pa. Deposition rate: 17 Å/min.
 40. **Evaporation of nickel:** The wafer is first clean in a argon plasma at P=100 W in 5 minutes whereafter 300 Å nickel is evaporated on the wafer without breaking the vacuum.

41. **Lift-off:** The metal is lifted in a ultrasonic acetone holder
42. **KOH etch of channels:** KOH etch of the wafers at 70 °C. Etch time: 70 min. Etch rate: $\sim 42 \mu\text{m}/\text{hour}$; $\sim 0.7 \mu\text{m}/\text{min}$.
43. **Etch of TEOS:** The rest of the TEOS is etched in BHF in 2 min.
44. **Evaporation of contact metal:** 100 Å Ti + 5000 Å Al is evaporated on the wafers
45. **Resist:** 4.2 μm resist is spun on the frontside of the wafers.
Photolithography: Mask 7 (contac. metal) is placed in the aligner. Aligner settings: prox, Expose with UV light for 150 sec ($7.1 \text{ mW}/\text{cm}^2$). The wafers is developed in a 1 AZ 351B : 5 DI water solution for 5 min at 22 °C.
46. **Etch of Al:** The Al is etched in the development solution.
47. **Etch of Ti:** The Ti is etched in a diluted BHF solution 1:5 BHF: H₂O
48. **Baking of the wafers:** The wafers are baked at 250 °C in 60 min
49. **SU-8:** The SU-8 XP 50 is spun on the wafers at 2500 rpm. Wait 5 min and repeat the whole step. Wait 15 minutes
50. **Prebake:** The SU-8 is prebaked on a hotplate at 70 °C for 50 minutes. The wafer is cooled down on the hotplate
51. **Photolithography:** Mask 8 (SU-8) is placed in the aligner. Aligner settings: prox, Expose with UV light at a dose of $620 \text{ mJ}/\text{cm}^2$.
52. **Postbake:** The wafers are baked on a hotplate at 70 °C in 50 min, the wafer is cooled down on the hotplate.
53. **Development:** The wafers are developed in PGMEA in 2x5 min and rinsed in 2-propanyl
54. **Hardbake:** The wafer is hardbaked in a convection oven at 95 °C for 30 minutes.

Appendix C

Summary

"Micro Total Analysis Systems" (μ TAS) is being used to identify devices including micro fluid handling. A μ TAS ideally is a system in which all steps from sample preparation to data representation are integrated in one instrument. The idea is actually to miniaturize a whole laboratory down on the chip, and the μ TAS concept is therefore also called "Lab on chip". One of the major issues in such devices is to integrate small but very sensitive sensors onto the chip.

This thesis describes a cantilever-based biochemical sensor integrated into a micro liquid handling system. The cantilevers have integrated piezoresistive elements as detection scheme. Cantilever-based bio chemical sensing using an external optical readout scheme gets complicated when measuring on an array of cantilevers. Also measurement on samples with changing refractive indices or even non-transparent liquids is complicated using the optical readout scheme. These problems are solved by using the integrated readout scheme.

A theory concerning the sensitivity of the surface stress sensitive cantilever-based sensor is developed. The most surprising results are that the sensitivity only depends on the cantilever material's stiffness and the total cantilever thickness. Furthermore the theory explains that the piezoresistor has to be placed on the same side of the neutral axis as the acting surface stress in order to obtain the highest sensitivity.

In order to optimize the performance of the sensor, the silicon piezoresistor was optimized with respect to signal to noise ratio. The parameters investigated were the doping concentration, annealing temperature and the grain size of the silicon. As expected using single crystalline silicon as the piezoresistor gives the highest performance, but due to the fact that poly silicon is easier to microfabricate, poly silicon material was used as the piezoresistive material in this thesis.

A design including 10 cantilevers in a micro liquid handling system is suggested. Wheatstone bridge configurations consisting of two cantilever resistors and two substrate resistors are used in the design. An *on-chip* mechanical filter is thereby obtained since the signal from the reference cantilever can be used for common mode rejection

of the signal from the measurement cantilever.

A processing sequence of the chip has been developed and the chip has been fabricated. Two versions of the chips have been realized. The first fabrication version has been made in order to test the processing sequence. Based on the experiences obtained from the processing and characterization of the first chip version a second optimized version of the chip has been realized. This version also includes an enhanced performance of the *on*-chip filter.

The first experiments performed with the chip include measurement on build-in stress in a nickel and a gold film. Furthermore, the gold coated measurement cantilevers have been used to detect the immobilization of molecules including a sulphur molecule. The experiments have been performed on octadecanethiol, cysteine and thiol-modified oligos. Due to the very sensitive sensing principle it has been possible to detect sub-monolayer formation on the cantilever.

Appendix D

Dansk resume

”Mikro Total Analyse Systemer” (μ TAS) anvendes som beskrivelse af apparater som indeholder mikrovæskehåndtering. Et μ TAS er ideelt set et system hvor alle trin, fra prøveforberedelse til dataopsamling er samlet i et instrument. Ideen er faktisk at formindske et helt laboratorium ned på en chip, og derfor er μ TAS-konceptet også kaldet ”Lab on chip”. En af de største udfordringer i sådant et apparat er at integrere en lille, men meget følsom sensor.

Denne afhandling omhandler en bjælke-baseret biokemisk sensor som er integreret ind i et mikrovæskehåndteringssystem. Bjælkerne har integrerede piezomodstande der anvendes som målemekanisme. Udlæsningen fra en bjælkebaseret biokemisk sensor, der anvender ekstern optisk udlæsning bliver kompliceret når der måles på flere bjælker. Målinger i væske som skifter brydningsindex eller er ugenomsigtige kompliceres også ved optisk udlæsning. Disse problemer er løst ved at bruge integreret udlæsning.

Der er blevet udarbejdet en teori, som beskriver virkemåden for den overfladestress følsomme bjælkebaserede sensor. De mest overraskende resultater er, at følsomheden kun afhænger af bjælkematerialets stivhed og bjælkens totale tykkelse. Der ud over forklarer teorien også, at den maksimale følsomhed opnås ved at placere piezomodstanden på samme side af den neutrale akse som det virkende overfladestress.

De piezoresistive siliciummodstanden er blevet undersøgt med hensyn til signal/støj forhold for at optimere sensoren. De undersøgte parametre er doteringskoncentration, varmebehandlingstemperatur og siliciumkornstørrelsen. Enkeltkrystallinsk silicium udviste som forventet det højeste signal/støj forhold, men da polykrystallinsk silicium er lettere at arbejde med i mikrofremstilling, anvendes dette som piezomodstandsmateriale i denne afhandling.

Et design bestående af 10 bjælker i et mikrovæskehåndteringssystem er foreslået. Wheatstonebrokonfigurationer bestående af to bjælke-modstande samt to substratmodstande er anvendt i dette design. Herved opnås et *on-chip* mekanisk filter, da signalet fra referencebjælken kan anvendes som en ”common mode rejection” af signalet fra målebjælken.

En fremstillingssekvens for chippen er blevet udviklet og på baggrund af denne er der blevet fremstillet chips. To fremstillingsforløb er blevet realiseret. Det første fremstillingsforløb blev foretaget for at teste fremstillingen. Baseret på de erfaringer der blev gjort ved det første fremstillingsforløb, samt karakteriseringen af de første chips blev der fremstillet en ny og optimeret generation af chips. Denne generation indeholder også en forbedring af *on-chip* filteret.

De første eksperimenter opnået med chippen inkluderer målinger af indbygget stress i nikkel- og guldfilm. Derudover har den guldbelagte målebjælke været anvendt til måling af immobilisering af molekyler der indeholder svovlatomer. Der er blevet foretaget eksperimenter med octadecanethiol, cysteine og thiol-modificeret oligoer. På grund af det meget følsomme måleprincip har det været muligt at måle sub-monolags formation på bjælken.